

SOM610 DVK

Hardware Guide

Version 0.4

© 2021 InSignal Co., Ltd. All rights reserved.



Important Notice

InSignal Co. Ltd. ("InSignal") reserves the right to make changes to the information in this publication at any time without prior notice. All information provided is for reference purpose only. InSignal assumes no responsibility for possible errors or omissions, or for any consequences resulting from the use of the information contained herein.

This publication on its own does not convey any license, either express or implied, relating to any InSignal and/or third-party products, under the intellectual property rights of InSignal and/or any third parties.

InSignal makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does InSignal assume any liability arising out of the application or use of any product or circuit and specifically disclaims any and all liability, including without limitation any consequential or incidental damages.

Customers are responsible for their own products and applications. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by the customer's technical experts.

InSignal products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the InSignal product could reasonably be expected to create a situation

where personal injury or death may occur. Customers acknowledge and agree that they are solely responsible to meet all other legal and regulatory requirements regarding their applications using InSignal products notwithstanding any information provided in this publication. Customer shall indemnify and hold InSignal and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, expenses, and reasonable attorney fees arising out of, either directly or indirectly, any claim (including but not limited to personal injury or death) that may be associated with such unintended, unauthorized and/or illegal use.

WARNING No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electric or mechanical, by photocopying, recording, or otherwise, without the prior written consent of InSignal. This publication is intended for use by designated recipients only. This publication contains confidential information (including trade secrets) of InSignal protected by Competition Law, Trade Secrets Protection Act and other related laws, and therefore may not be, in part or in whole, directly or indirectly publicized, distributed, photocopied or used (including in a posting on the Internet where unspecified access is possible) by any unauthorized third party. InSignal reserves its right to take any and all measures both in equity and law available to it and claim full damages against any party that misappropriates InSignal's trade secrets and/or confidential information.

Copyright © 2021 InSignal Co., Ltd.

InSignal Co., Ltd.
#1104, Byucksan Digital Valley 7st., 50 Digital-ro 33gil Guro-gu, Seoul
08377, Rep. of KOREA

Home Page: <http://www.insignal.co.kr>

Trademarks

All brand names, trademarks and registered trademarks belong to their respective owners.

- ARM, Jazelle, TrustZone, and Thumb are registered trademarks of ARM Limited. Cortex, ETM, ETB, Coresight, ISA, and Neon are trademarks of ARM Limited.
- Java is a trademark of Sun Microsystems, Inc.
- SD is a registered trademark of Toshiba Corporation.
- MMC and eMMC are trademarks of MultiMediaCard Association.
- JTAG is a registered trademark of JTAG Technologies, Inc.
- Synopsys is a registered trademark of Synopsys, Inc.
- I2S is a trademark of Phillips Electronics.
- I2C is a trademark of Phillips Semiconductor Corp.
- MIPI and Slimbus are registered trademarks of the Mobile Industry Processor Interface (MIPI) Alliance.

All other trademarks used in this publication are the property of their respective owners.

Table of Contents

1 INTRODUCTION	1
1.1 Purpose and Scope	1
1.2 Version	1
2 DOCUMENTS	2
2.1 Reference Documents.....	2
3 MECHANICAL AND ELECTRICAL DESIGN GUIDELINES	3
3.1 Mechanical Design for SOM610.....	3
3.2 SOM610 Mechanical Outline.....	3
3.3 Top and Bottom Height Restrictions of SOM610.....	5
3.4 Electrical absolute maximum value	5
3.5 Electrical operating condition	5
3.6 Connectors for SOM610	6
3.6.1 Board-to-board Connectors of Bottom Side of SOM610	6
3.6.2 Board-to-Board Connectors Ordering and Orientation	7
3.6.3 Pin Map of SOM610 Connectors	8
3.6.4 RF Antenna Connectors.....	15
4 USAGE OF DVK	16
4.1 Anti-Static Handling Procedures.....	16
4.2 SOM610 DVK Hardware Specifications	16
4.2.1 SOM610 Block Diagram & specifications	16
4.2.2 SOM610 DVK Hardware Block Diagram & Specifications	18
4.3 SOM610 DVK Hardware Port Description.....	20
4.3.1 USB A CONNECTOR, CN7.....	22
4.3.2 Debug UART PIN Header, J8 (NOT implemented).....	22
4.3.3 RS-232 Debug Connector, CON3	23
4.3.4 Power On/Off Toggle Switch, SW6	24
4.3.5 DC Power Input Adaptor Jack, CON1	25
4.3.6 Boot Option Pin Header, J4	26
4.3.7 USB_CC1 Jumper Pin Header, J15	26
4.3.8 USB-C Connector, CN6	28
4.3.9 HDMI Output Connector, CN4	30
4.3.10 MIPI CSI Camera PIN Headers, J10, J12, J11	30
4.3.11 3- Color LED PIN Header, J5 (NOT implemented).....	34
4.3.12 Home Key and H/W Reset Pin Headers, J16, J17 (NOT implemented)	35
4.3.13 Key Button Tact Switches, SW1, SW2, SW3	36
4.3.14 Antenna Connectors, CON4 ~ CON7	37
4.3.15 Micro SD Card Slot, CON8.....	38
4.3.16 Analog Headset Phone Jack Connector, CON10	39
4.3.17 Analog Speaker Output Connector, CON9	39
4.3.18 Analog Microphone, MIC1	40
4.3.19 GPIO Pin Header J6, J7.....	40

4.3.20 Microprocessor GPIOs PIN Header, J14.....	42
4.3.21 Microprocessor F/W download PIN Header, J13 (Not Implemented)	42
4.3.22 DP Output PIN Header, J9	42
4.3.23 Ethernet RJ45 Connector, CN5	43
4.3.24 DVK Main Power Selection Jumper PIN Header, J3.....	43
4.3.25 Battery Power, J2 (Not Implemented).....	44
4.3.26 DC to Battery Power Jumper PIN Header, J1	46
4.3.27 Summary : Default Board Jumper Setting, J1, J3, J4, J5	47

List of Figures

Fig. 3-1 Top View of SOM610 (Default) top side	3
Fig. 3-2 Top View of SOM610 (Option : CAN type) top side.....	4
Fig. 3-3 Dimensions for Top View of SOM610 Bottom Side	4
Fig. 3-4 Board-to-Board Connectors of SOM610	6
Fig. 3-5 Pin Ordering.....	7
Fig. 3-6 Connector locations of Top View for Bottom Side	7
Fig. 3-7 RF Antenna Connector Part Name of SOM610	15
Fig. 4-1 Abstract functional block diagram of SOM610	17
Fig. 4-2 SOM610 DVK block diagram	19
Fig. 4-3 Outline Diagram of SOM610 DVK V1.1	20
Fig. 4-4 Circuits about CN7	22
Fig. 4-5 Location of J8	22
Fig. 4-6 Circuits about J8	23
Fig. 4-7 Debug Serial RS232, DB-9 F Connector	23
Fig. 4-8 SW6 circuits of SOM610 DVK Carrier board.....	24
Fig. 4-9 Generation of MAIN_PWR_SRC from DC_IN	25
Fig. 4-10 Adaptor Jack Mechanical Drawing	25
Fig. 4-11 Set FORCED_USB_BOOT	26
Fig. 4-12 Default position of Jumper for J15	27
Fig. 4-13 USB_CC1 selection for J15	27
Fig. 4-14 Circuits for USB_CC2 signal.....	27
Fig. 4-15 Location of USB-C connector CN6.....	28
Fig. 4-16 USB-C Connector	29
Fig. 4-17 Location of HDMI connector.....	30
Fig. 4-18 Positions for MIPI CSI's	31
Fig. 4-19 Pins of Camera CSI#0 Pin Header, J10.....	31
Fig. 4-20 Pin position and orientation for J10	32
Fig. 4-21 Pins of Camera CSI #2 Pin Header, J12.....	32
Fig. 4-22 Pin position and orientation for J12	33
Fig. 4-23 Pins of Camera CSI #1 Pin Header, J11	33
Fig. 4-24 Pin position and orientation for J11	34
Fig. 4-25 Location for J5	34
Fig. 4-26 Pins for J5	35
Fig. 4-27 Pin Headers of Key Home & HW Reset.....	35
Fig. 4-28 Locations of SW1, SW2 and SW3.....	36
Fig. 4-29 Signals for SW1, SW2 and SW3	36
Fig. 4-30 WIFI/BT SMA Connector.....	38

Fig. 4-31 micro-SD Card slot, CON8.....	38
Fig. 4-32 Circuits of Headset Jack, CON10	39
Fig. 4-33 Analog Sound Outputs, CON9 and CON10.....	39
Fig. 4-34 Location of Microphone, MIC1	40
Fig. 4-35 Signals of J6 and J7.....	41
Fig. 4-36 Locations of J6 and J7.....	41
Fig. 4-37 DP Pin Header, J9	42
Fig. 4-38 Location of J9	42
Fig. 4-39 Location of CN5, RJ45 Connector.....	43
Fig. 4-40 Pin Header, J3	44
Fig. 4-41 Location of Battery Connector J2	44
Fig. 4-42 Circuits of Pin Header J2	45
Fig. 4-43 Generating VBATT_CONN from DC_IN	46
Fig. 4-44 Location of J1	46
Fig. 4-45 Default Board Jumpers.....	47

1 Introduction

1.1 Purpose and Scope

The purpose of this document is to provide basic information about the SOM610 module, as well as user guide for the DVK with this module. In particular, it is to help to develop or evaluate hardware and software using SOM610 module.

In addition, SOM610 DVK itself is not a certified product, it is only a board used to evaluate and check to develop a product, and its main purpose is to confirm for its availability for functional operation.

Therefore, InSignal doesn't have the responsibility for all problems arising from application directly to the product or remodeling or using for commercial purposes, as well as the responsibility for product life, failure, and overload caused by repeating the act of frequently attaching and detaching SOM610 module, and by applying load to the SOM610 module. InSignal is only suggesting, not forcing it.

In addition, since DVK of our company is especially provided for various tests and evaluations, we cannot guarantee anything that is deliberately or neglected by the user, deviating from the usage method prescribed by each country, particularly in the case that the method of use for radio frequency is outside the regulations of each country, or in the method of using power or other safety standards and dangers.

The purpose of this document is to provide guidelines and technical information for any user desiring to design their own Carrier Board for the InSignal System On Module (SOM).

1.2 Version

In addition, the guidelines of this document may be modified or changed depending on the hardware and software of SOM610 module or DVK Carrier. The currently sold hardware versions are as follows.

SOM610	V1.0
SOM610 DVK Carrier	V1.1

2 Documents

In this chapter, documents related to SOM610 are listed. Qualcomm and third-party documents that are not mentioned are not provided in this document and materials.

This Chapter lists any parent and supplementary documents for the SOM610 Development Kit User Guide. Unless stated otherwise, applicable documents supersede this document and reference documents provide background and actual data.

2.1 Reference Documents

Documents or materials provided

SOM610 DVK carrier Board Schematics	ORCAD DSN file and PDF file of DVK board
SOM610 DVK carrier Board Layout	PADS Layout PCB file of DVK board
SOM610 DVK carrier Board DXF files	DXF file for CAD to check SOM610 pin placement and size on DVK board
SOM610 DVK carrier Board BOM	Bill of Material file of DVK board
SOM610 Pin Map	Excell file of the signals name for SOM610 connectors

3

Mechanical and Electrical Design Guidelines

3.1 Mechanical Design for SOM610

This chapter refers to the mechanical data of the module itself required when developing using SOM610 module. The color and version information of the PCB among the appearance of the actual module can be arbitrarily changed according to production, but the outer size of the module, pin map information and direction information of the connector are not changed.

SOM610 Development Kit provides reference materials to help customers design, develop, test and build the robustness of Qualcomm's QCS610 processors in their product solutions, on the condition that they utilize the SOM610 equipped with the Qualcomm QCS610 processor. This section describes mechanical design guidelines for developing customized carrier boards for SOMs.

3.2 SOM610 Mechanical Outline

The physical outline and dimensions of the SOM610 are shown in the figures below:

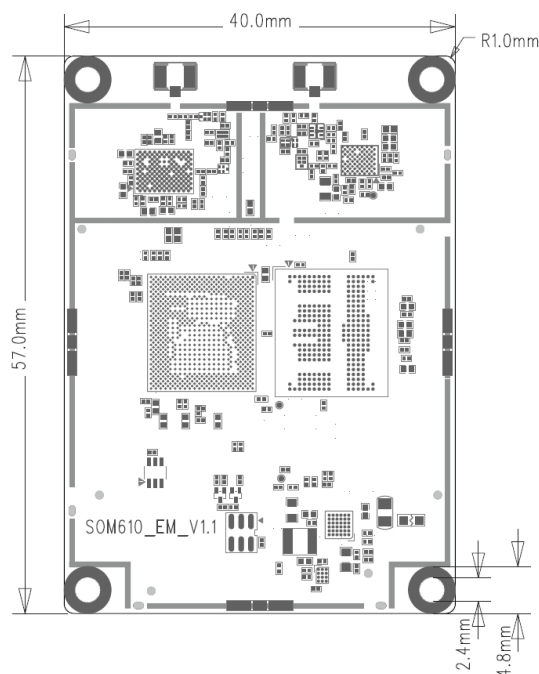


Fig. 3-1 Top View of SOM610 (Default) top side

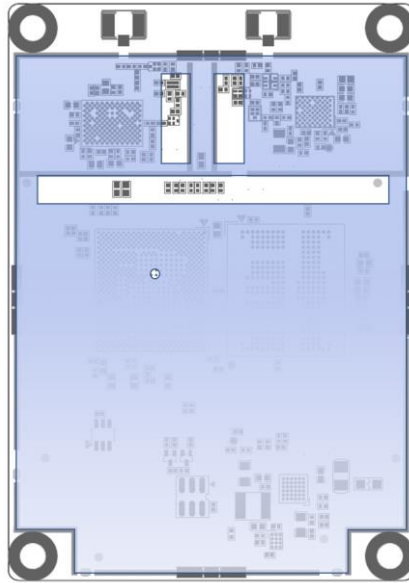


Fig. 3-2 Top View of SOM610 (Option : CAN type) top side

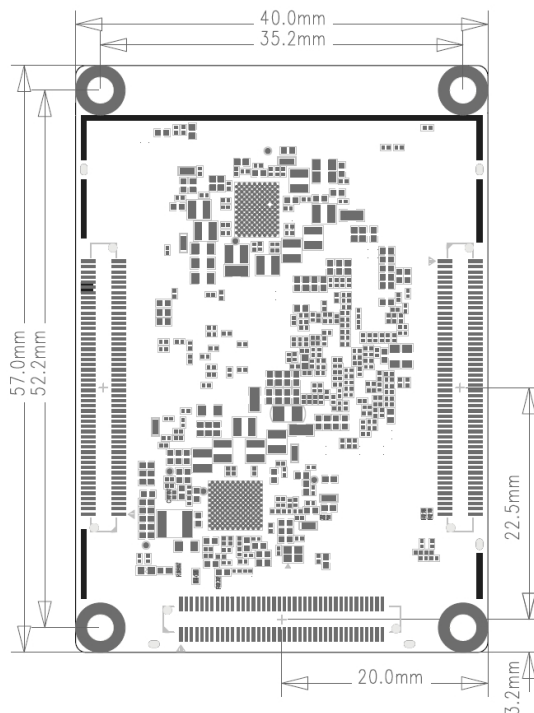


Fig. 3-3 Dimensions for Top View of SOM610 Bottom Side

Please contact us for the SOM shield CAN installation. Also, it can be changed according to the production schedule.

3.3 Top and Bottom Height Restrictions of SOM610

The highest part of SOM610 without a shield CAN is 1.6mm. If the CAN is mounted, the height to the CAN is 2.2mm. And the shield CAN is not mounted on the bottom side, but since the height of the highest part on the bottom side is 1.3mm, it is forbidden to place the parts on the carrier board in the position just below the SOM module so that the parts do not interfere with the assembly.

The stacking height between Carrier Board and the SOM depends on the connector used in the Carrier board. SOM610 Carrier board uses connector with 2.5mm stacking height. It is recommended that there be no components placed in the area on the Carrier Board underneath the SOM when stacking height between the Carrier Board and SOM is 1.5mm.

3.4 Electrical absolute maximum value

The input power of the DVK carrier board is available with either an adapter power supply or a USB C power supply. Therefore, the Absolute Condition in Table 3-1 must be satisfied.

Table 3-1 Absolute Condition

Description	Symbol Name	Min.	Typ.	Max.
USB-C USB VBUS	USB_VBUS_CONN	-0.3		16
Adaptor Jack Power Voltage	DCIN	-0.3	--	15

3.5 Electrical operating condition

DVK's operating voltage is as shown in Table 3-2 Operation Power Condition below.

Table 3-2 Operation Power Condition

Description	Symbol Name	Min.	Typ.	Max.
USB-C USB VBUS [V]	USB_VBUS_CONN	4.7	--	14
Adaptor Jack Power Voltage [V]	DCIN	4.7	--	14
Adaptor Jack Power Ampere [A]	DCIN	2.0	--	3.0

3.6 Connectors for SOM610

3.6.1 Board-to-board Connectors of Bottom Side of SOM610

The SOM610 mounts to the SOM610 DVK board through two 100-pin and one 80-pin board to board connectors. Customers that are designing their own carrier board must ensure that their connector pinouts match the ones on the SOM610 DVK schematics.

The connectors fitted to the AXK6F00337YG are from Panasonic, and the connectors corresponding to Panasonic's AXK6F00337YG are provided according to the combined height, but SOM610 only supports one of the height constraints mentioned in section 3.3. Apply Panasonic Corp.'s AXK5F00547YG to the Carrier Board connector as shown in the Table 3-3 below.

Table 3-3 Carrier Board Connector for SOM610

	SOM610	Carrier Board	Stacking Mated Height	Recommend
Connector	AXK6F00337YG	AXK5F00547YG	2.5mm	Yes

The Fig. 3-4 below shows the location of the Board-to-board connector on the SOM610.

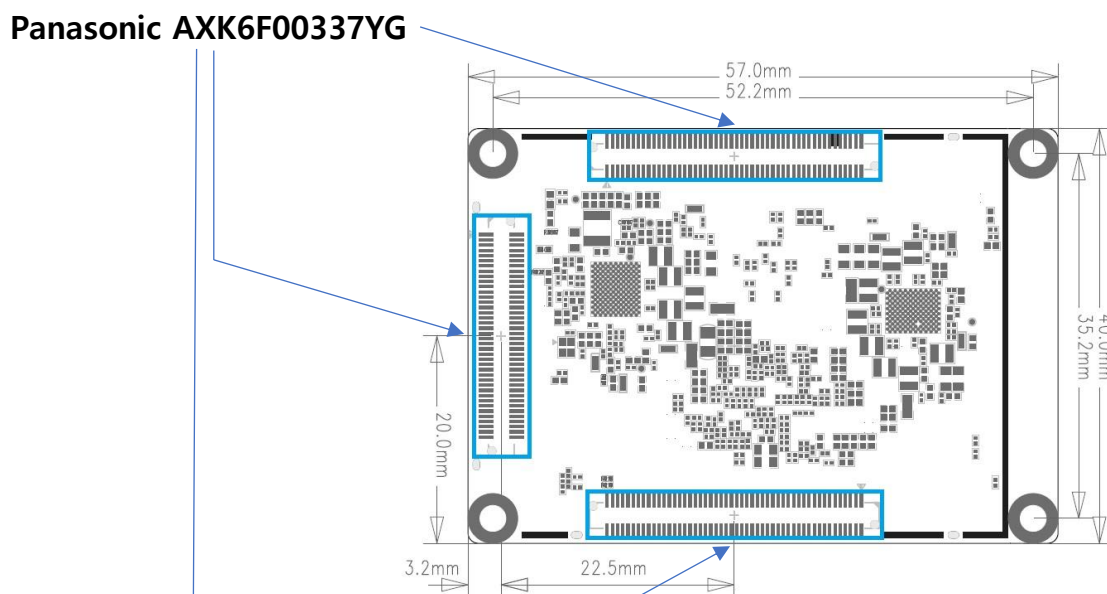


Fig. 3-4 Board-to-Board Connectors of SOM610

The exact locations of the connectors during design are shown in Fig. 3-4. In actual design, the DXF file of SOM610 Carrier Board is provided.

3.6.2 Board-to-Board Connectors Ordering and Orientation

Connector pin order is allocated in the left and right zigzag direction.

The pin order of the Board-to-board connectors is numbered from 1 to zigzag as shown in the Fig. 3-5 below.

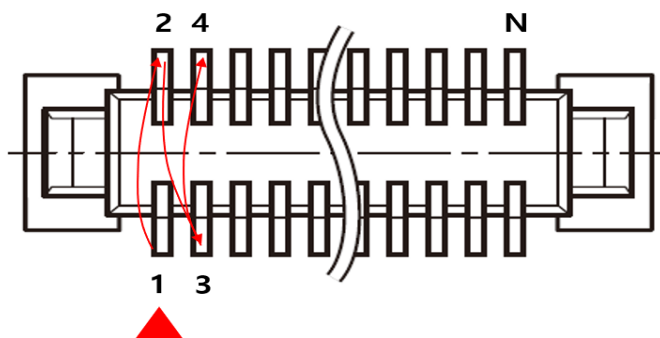


Fig. 3-5 Pin Ordering

The location of the connectors and pin No. 1 is shown in Fig. 3-6 below.

TOP VIEW of Bottom Side

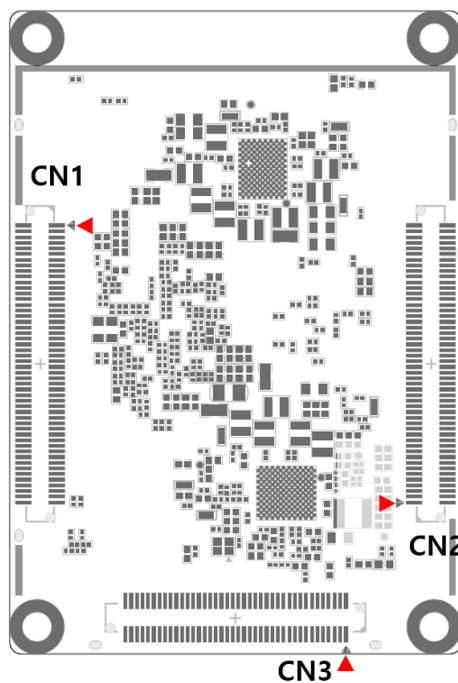


Fig. 3-6 Connector locations of Top View for Bottom Side

3.6.3 Pin Map of SOM610 Connectors

As the connector of the counterpart required by SOM610 described in Chapter 3, AXK5F00547YG was used among the connectors mentioned in Table 3-3. When this connector is combined with SOM610, the stacking height with the carrier board is 2.5mm. When designing and manufacturing a carrier board using the SOM610 module, the user should not place other parts on the top surface just below the SOM610, and make sure not to cause problems caused by contacting parts and parts during actual assembly and bonding.

As described in Chapter 3, there are 3 Board-to-board connectors in the SOM610. For information on the position, orientation and numbering of the pins for the connectors, see section 3.6.2. This section describes the pins of the connectors.

3.6.3.1 CN1

#	Pin Name	Power	IN/OUT	Description
1	GP0_QUP0_2_0_I2C_SDA	1.8V	I/O	GPIO0 of QCS610, use QUP0_2
3	GP1_QUP0_2_1_I2C_SCL	1.8V	I/O	GPIO1 of QCS610, use QUP0_2
5	GP2_QUP0_2_2	1.8V	I/O	GPIO2 of QCS610, use QUP0_2
7	GP3_QUP0_2_3	1.8V	I/O	GPIO3 of QCS610, use QUP0_2
9	GP4_QUP0_1_I2C_SDA	1.8V	I/O	GPIO4 of QCS610, use QUP0_1
11	GP5_QUP0_1_I2C_SCL	1.8V	I/O	GPIO5 of QCS610, use QUP0_1
13	GP6_QUP1_2_SPI_MISO	1.8V	I/O	GPIO6 of QCS610, use QUP1_2
15	GP7_QUP1_2_SPI_MOSI	1.8V	I/O	GPIO7 of QCS610, use QUP1_2
17	GP8_QUP1_2_SPI_SCLK	1.8V	I/O	GPIO8 of QCS610, use QUP1_2
19	GP9_QUP1_2_SPI_CS_N	1.8V	I/O	GPIO9 of QCS610, use QUP1_2
21	GP14_QUP1_1_I2C_SDA	1.8V	I/O	GPIO14 of QCS610, use QUP1_1, I2C data
23	GP15_QUP1_1_I2C_SCL	1.8V	I/O	GPIO15 of QCS610, use QUP1_1, I2C clock
25	GND		I	
27	GP18_QUP0_3_I2C_SDA	1.8V	I/O	GPIO18 of QCS610, use QUP0_3, I2C data
29	GP19_QUP0_3_I2C_SCL	1.8V	I/O	GPIO19 of QCS610, use QUP0_3, I2C clock
31	GP20_QUP1_0_0_CTSN	1.8V	I/O	GPIO20 of QCS610, use QUP1_0
33	GP21_QUP1_0_1_RTSN	1.8V	I/O	GPIO21 of QCS610, use QUP1_0
35	GP22_QUP1_0_2_UTXD	1.8V	I/O	GPIO22 of QCS610, use QUP1_0
37	GP23_QUP1_0_3_URXD	1.8V	I/O	GPIO23 of QCS610, use QUP1_0
39	LPI0_I2C_SDA		I/O	
41	LPI0_I2C_SCL		O	
43	LPI1_SPI_MISO		I	
45	LPI1_SPI_MOSI		O	
47	LPI1_SPI_CLK		I	
49	LPI1_SPI_CSN0		O	
51	LPI1_SPI_CSN1		O	
53	GND		I	
55	GND		I	

Guidelines

57	LPI2_SPI_MISO		I	
59	LPI2_SPI_MOSI		O	
61	LPI2_SPI_CLK		I	
63	LPI2_SPI_CSN		O	
65	GND		I	
67	GND		I	
69	GND		I	
71	GND		I	
73	GND		I	
75	LPIGP26_DMIC_CLK1	1.8V	I/O	GPIO26 of QCS610, use LPI
77	LPIGP27_DMIC_DATA1	1.8V	I/O	GPIO27 of QCS610, use LPI
79	LPIGP28_DMIC_CLK2	1.8V	I/O	GPIO28 of QCS610, use LPI
81	LPIGP29_DMIC_DATA2	1.8V	I/O	GPIO29 of QCS610, use LPI
83	GND	1.8V	I	
85	GP66	1.8V	I/O	GPIO66 of QCS610
87	GP69	1.8V	I/O	GPIO69 of QCS610
89	GP71_MPMI	1.8V	I/O	GPIO71 of QCS610
91	GP74	1.8V	I/O	GPIO74 of QCS610
93	GP76_ETH_PHY_INT_N	1.8V	I	GPIO76 of QCS610, Ethernet PHY INT
95	GP89_MPMI	1.8V	I/O	GPIO89 of QCS610
97	GP91_MPMI	1.8V	I/O	GPIO91 of QCS610
99	GP100_MPMI	1.8V	O	GPIO100 of QCS610

#	Pin Name	Power	IN/OUT	Description
2	VREG_L6C_SDC2		O	
4	VREG_L9C_2P95		O	
6	VREG_L9C_2P95		O	
8	PMB_GP5_AMUX	1.8V	I/O	GPIO5 of PM6150L
10	GND		I	
12	PMA_GP8_AMUX2	1.8V	I/O	GPIO8 of PM6150
14	GP111	1.8V	I/O	GPIO111 of QCS610, TW5001 Reset
16	GP119_MPMI	1.8V	I/O	GPIO119 of QCS610
18	GND		I	
20	SDC2_CLK		O	SD Card CLK
22	SDC2_CMD		O	SD Card CMD
24	SDC2_DATA_0		I/O	SD Card DATA 0
26	SDC2_DATA_1		I/O	SD Card DATA 1
28	SDC2_DATA_2		I/O	SD Card DATA 2
30	SDC2_DATA_3		I/O	SD Card DATA 3
32	GND		I	
34	GP85_MPMI_GYRO_DRDY_INT	1.8V	I	GPIO85 of QCS610, GYRO Data Ready INT
36	GP86_MPMI_GYRO_EVENT_INT	1.8V	I	GPIO86 of QCS610, GYRO Event INT

Guidelines

38	GP121_MI2S_2_MCLK	1.8V	O	GPIO121 of QCS610, MI2S MCLK
40	GP115_MI2S_2_SCK	1.8V	I/O	GPIO115 of QCS610, MI2S SCK
42	GP116_MI2S_2_WS	1.8V	I/O	GPIO116 of QCS610, MI2S WS
44	GP117_MI2S_2_DATA0	1.8V	O	GPIO117 of QCS610, MI2S DATA0
46	GP118_MI2S_2_DATA1	1.8V	I	GPIO118 of QCS610, MI2S DATA1
48	GND		I	
50	GP24	1.8V	I/O	GPIO24 of QCS610
52	GP25	1.8V	I/O	GPIO25 of QCS610
54	GP26_HDMI_INT	1.8V	I	GPIO26 of QCS610, HDMI INT
56	GP31	1.8V	I	GPIO31 of QCS610, Earjack DET
58	GP36_ETH_PHY_RST_N	1.8V	O	GPIO36 of QCS610, Ethernet PHY Reset
60	GP37	1.8V	I/O	GPIO37 of QCS610
62	GP38	1.8V	I/O	GPIO38 of QCS610
64	GP40	1.8V	I/O	GPIO40 of QCS610
66	GP41_MPMI	1.8V	I/O	GPIO41 of QCS610
68	GP42	1.8V	I/O	GPIO42 of QCS610
70	GP44_MPMI	1.8V	I	GPIO44 of QCS610, Audio INT
72	GND		I	
74	GP49	1.8V	I/O	GPIO49 of QCS610
76	GP50_MPMI	1.8V	I/O	GPIO50 of QCS610
78	GP53	1.8V	I/O	GPIO53 of QCS610
80	GP58	1.8V	O	GPIO58 of QCS610, LT9611 Reset
82	GP59_GPCLK3A	1.8V	I/O	GPIO59 of QCS610, GP Clock
84	GP60_MPMI	1.8V	I/O	GPIO60 of QCS610
86	GP64	1.8V	I/O	GPIO64 of QCS610
88	GP68	1.8V	I/O	GPIO68 of QCS610
90	GP73	1.8V	I/O	GPIO73 of QCS610
92	GND		I	
94	GP78	1.8V	I/O	GPIO78 of QCS610, GP Clock
96	GP90_MPMI	1.8V	I/O	GPIO90 of QCS610
98	GP98_MPMI	1.8V	I/O	GPIO98 of QCS610
100	GP99_MPMI	1.8V	I	GPIO99 of QCS610, SD Card DET

3.6.3.2 CN2

#	Pin Name	Power	IN/OUT	Description
1	VBATT_CONN		I	
3	VBATT_CONN		I	
5	VBATT_CONN		I	
7	VREG_L4C_1P8	1.8V	O	
9	VREG_L5C_1P8	1.8V	O	
11	VREG_L8C_1P8	1.8V	O	
13	GND		I	

Guidelines

15	CAM_MCLK0		O	CAM MCLK0
17	CAM_MCLK1		O	CAM MCLK1
19	CAM_MCLK2		O	CAM MCLK2
21	GND		I	
23	PMB_GP3_CAM_PWR_EN		O	GPIO3 of PM6150L, CAM Power Enable
25	PMB_GP4_CAM_PWR_EN		O	GPIO4 of PM6150L, CAM Power Enable
27	PMB_GP9_CAM_PWR_EN		O	GPIO9 of PM6150L, CAM Power Enable
29	GP45_CAM1_RST_N		O	GPIO45 of QCS610, CAM1 Reset
31	GP46		I/O	GPIO46 of QCS610, CAM2 Reset
33	GP47_CAM0_RST_N		O	GPIO47 of QCS610, CAM0 Reset
35	GND		I	
37	MIPI_CSI0_CLK_P		I	MIPI CSI0 Clock
39	MIPI_CSI0_CLK_M		I	MIPI CSI0 Clock
41	GND		I	
43	MIPI_CSI0_LANE0_P		I	MIPI CSI0 LANE 0-
45	MIPI_CSI0_LANE0_M		I	MIPI CSI0 LANE 0-
47	GND		I	
49	MIPI_CSI0_LANE1_P		I	MIPI CSI0 LANE 1-
51	MIPI_CSI0_LANE1_M		I	MIPI CSI0 LANE 1-
53	GND		I	
55	MIPI_CSI0_LANE2_P		I	MIPI CSI0 LANE 2-
57	MIPI_CSI0_LANE2_M		I	MIPI CSI0 LANE 2-
59	GND		I	
61	MIPI_CSI0_LANE3_P		I	MIPI CSI0 LANE 3-
63	MIPI_CSI0_LANE3_M		I	MIPI CSI0 LANE 3-
65	GND		I	
67	CCI_I2C_SCL0		O	CAM I2C0 Clock
69	CCI_I2C_SDA0		I/O	CAM I2C0 Data
71	GND		I	
73	MIPI_CSI1_CLK_P		I	MIPI CSI1 Clock
75	MIPI_CSI1_CLK_M		I	MIPI CSI1 Clock
77	GND		I	
79	MIPI_CSI1_LANE0_P		I	MIPI CSI1 LANE 0-
81	MIPI_CSI1_LANE0_M		I	MIPI CSI1 LANE 0-
83	GND		I	
85	MIPI_CSI1_LANE1_P		I	MIPI CSI1 LANE 1-
87	MIPI_CSI1_LANE1_M		I	MIPI CSI1 LANE 1-
89	GND		I	
91	MIPI_CSI1_LANE2_P		I	MIPI CSI1 LANE 2-
93	MIPI_CSI1_LANE2_M		I	MIPI CSI1 LANE 2-
95	GND		I	
97	MIPI_CSI1_LANE3_P		I	MIPI CSI1 LANE 3-
99	MIPI_CSI1_LANE3_M		I	MIPI CSI1 LANE 3-

Guidelines

#	Pin Name	Power	IN/OUT	Description
2	VBATT__CONN		I	
4	VBATT__CONN		I	
6	VBATT__CONN		I	
8	VBATT__CONN		I	
10	GND		I	
12	GND		I	
14	MIPI_DSI0_CLK_P		O	MIPI DSI0 Clock
16	MIPI_DSI0_CLK_M		O	MIPI DSI0 Clock
18	GND		I	
20	MIPI_DSI0_LANE0_P		O	MIPI DSI0 LANE 0-
22	MIPI_DSI0_LANE0_M		O	MIPI DSI0 LANE 0-
24	GND		I	
26	MIPI_DSI0_LANE1_P		O	MIPI DSI0 LANE 1-
28	MIPI_DSI0_LANE1_M		O	MIPI DSI0 LANE 1-
30	GND		I	
32	MIPI_DSI0_LANE2_P		O	MIPI DSI0 LANE 2-
34	MIPI_DSI0_LANE2_M		O	MIPI DSI0 LANE 2-
36	GND		I	
38	MIPI_DSI0_LANE3_P		O	MIPI DSI0 LANE 3-
40	MIPI_DSI0_LANE3_M		O	MIPI DSI0 LANE 3-
42	GND		I	
44	CCI_I2C_SCL1		O	CAM I2C1 Clock
46	CCI_I2C_SDA1		I/O	CAM I2C1 Data
48	GND		I	
50	MIPI_CSI2_CLK_P		I	MIPI CSI2 Clock
52	MIPI_CSI2_CLK_M		I	MIPI CSI2 Clock
54	GND		I	
56	MIPI_CSI2_LANE0_P		I	MIPI CSI2 LANE 0-
58	MIPI_CSI2_LANE0_M		I	MIPI CSI2 LANE 0-
60	GND		I	
62	MIPI_CSI2_LANE1_P		I	MIPI CSI2 LANE 1-
64	MIPI_CSI2_LANE1_M		I	MIPI CSI2 LANE 1-
66	GND		I	
68	MIPI_CSI2_LANE2_P		I	MIPI CSI2 LANE 2-
70	MIPI_CSI2_LANE2_M		I	MIPI CSI2 LANE 2-
72	GND		I	
74	MIPI_CSI2_LANE3_P		I	MIPI CSI2 LANE 3-
76	MIPI_CSI2_LANE3_M		I	MIPI CSI2 LANE 3-
78	GND		I	
80	LED_RED		O	RGB_RED of PM6150L, RED LED
82	LED_GRN		O	RGB_GRN of PM6150L, GREEN LED
84	LED_BLU		O	RGB_BLU of PM6150L, BLUE LED

Guidelines

86	PMB_GP6_PWM	1.8V	O	GPIO6 of PM6150L
88	VPH_PWR		O	
90	VPH_PWR		O	
92	VPH_PWR		O	
94	VPH_PWR		O	
96	VPH_PWR		O	
98	CAM_FLASH1		O	FLASH_LED1 of PM6150L, CAM Flash
100	CAM_FLASH1		O	FLASH_LED1 of PM6150L

3.6.3.3 CN3

#	Pin Name	Power	IN/OUT	Description
1	DC_IN		I	
3	DC_IN		I	
5	DC_IN		I	
7	DC_IN		I	
9	DC_IN		I	
11	USB_VBUS_CONN		I	
13	USB_VBUS_CONN		I	
15	USB_VBUS_CONN		I	
17	USB_VBUS_CONN		I	
19	USB_VBUS_CONN		I	
21	VCOIN		O	Coin Battery Holder
23	uSD_BOOT		I	Micro SD Boot configuration
25	FORCED_USB_BOOT		I	USB Boot configuration
27	TYPEC_uUSB_SEL		I	
29	USB3_HS_DET_DP		I/O	USB3 HS DET
31	USB3_HS_DET_DM		I/O	USB3 HS DET
33	VREG_L19A_2P85	2.85V	O	Ethernet Power
35	VREG_L16A_3P3	3.3V	O	
37	GP110_MPMI	1.8V	I	GPIO110 of QCS610, INT
39	GND		I	
41	DBG_UART_RX		I	Debug UART RX
43	DBG_UART_TX		O	Debug UART TX
45	GND		I	
47	DP_AUX_M		O	DP AUX
49	DP_AUX_P		O	DP AUX
51	GND		I	
53	DP_L0_M		O	DP LANE 0
55	DP_L0_P		O	DP LANE 0
57	GND		I	
59	USB1_HS_DP		I/O	USB1 HS
61	USB1_HS_DM		I/O	USB1 HS

Guidelines

63	GND		I	
65	DP_L1_M		O	DP LANE 1
67	DP_L1_P		O	DP LANE 1
69	GND		I	
71	DP_L2_M		O	DP LANE 2
73	DP_L2_P		O	DP LANE 2
75	GND		I	
77	DP_L3_M		O	DP LANE 3
79	DP_L3_P		O	DP LANE 3

#	Pin Name	Power	IN/OUT	Description
2	BATT_THERM		I	
4	BATT_ID		I	
6	KEY_HOME_N		I	HOME Key, GPIO11 of PM6150L
8	PM_RESIN_N		I	RESET Key, RESIN_N of PM6150
10	KEY_VOLP_N		I	VOL+ Key, GPIO2 of PM6150L
12	PHONE_ON_N		I	PHONE ON Key, KPD_PWR_N of PM6150
14	USB_CC2		I	CC2 of PM6150, J15
16	USB_CC1		I	CC1_ID of PM6150, J15
18	USB_THERM		I	USB Thermal Check
20	HW_RESET_H		I	
22	GND		I	
24	USB3_SS_TX0_M		O	USB3 SS TX0
26	USB3_SS_TX0_P		O	USB3 SS TX0
28	GND		I	
30	USB3_SS_RX0_M		I	USB3 SS RX0
32	USB3_SS_RX0_P		I	USB3 SS RX0
34	GND		I	
36	USB3_SS_TX1_M		O	USB3 SS TX1
38	USB3_SS_TX1_P		O	USB3 SS TX1
40	GND		I	
42	USB3_SS_RX1_M		I	USB3 SS RX1
44	USB3_SS_RX1_P		I	USB3 SS RX1
46	GND		I	
48	USB3_HS_DP		I/O	USB3 HS
50	USB3_HS_DM		I/O	USB3 HS
52	GND		I	
54	GP83_RGMII_RXD0		I	RGMII RXD0
56	GP82_RGMII_RXD1		I	RGMII RXD1
58	GP81_RGMII_RXD2		I	RGMII RXD2
60	GP96_RGMII_TXD0		O	RGMII TXD0
62	GP95_RGMII_TXD1		O	RGMII TXD1

Guidelines

64	GP92_RGMII_GTX_CLK		O	RGMII Clock
66	GP97_RGMII_TX_EN		O	RGMII TX Enable
68	GP94_RGMII_TXD2		O	RGMII TXD2
70	GP93_RGMII_TXD3		O	RGMII TXD3
72	RGMII_RX_CLK		I	RGMII RX Clock, Never Pull-up
74	GP103_RGMII_RXD3		I	RGMII RXD3
76	GP114_RGMII_MDIO		I	RGMII MDIO
78	GP112_RGMII_RX_CTL		I	RGMII RX CTL
80	GP113_RGMII_MDC		I	RGMII MDC

3.6.4 RF Antenna Connectors

There are two RF antenna connectors. In the figure below, there are two antenna connector seats, but the GNSS connector and its functions are not supported in the actual product, and only WIFI/BT antenna connector is supported.

The SOM contains two IPEX coaxial receptacles (IPEX 20279-001E) for connecting to GNSS, and WLAN/BT RF antenna. Fig. 3-7 shows RF Antenna connectors located on the top surface of SOM610.

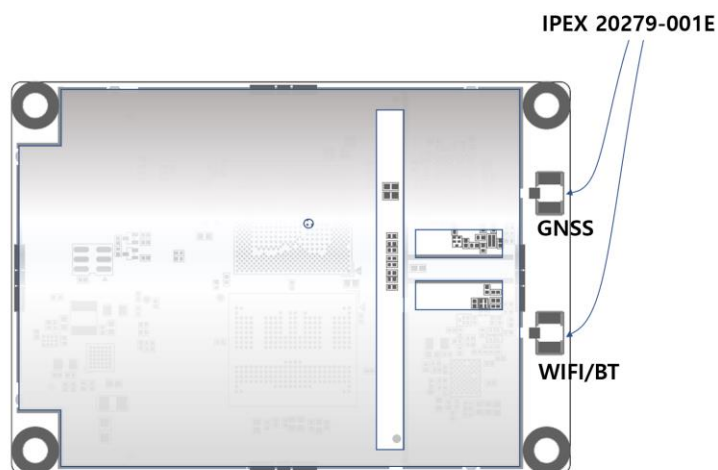


Fig. 3-7 RF Antenna Connector Part Name of SOM610

The antenna port of WIFI/BT supports both 2.4GHz and 5GHz.

4

Usage of DVK

This development platform contains RF/digital hardware and software intended for engineering development, engineering evaluation, or demonstration purposes only and is meant for use in a controlled environment. This device is not being placed on the market, leased or sold for use in a residential environment or for use by the general public as an end user device.

This development platform is not intended to meet the requirements of a commercially available consumer device including those requirements specified in the European Union directives applicable for Radio devices being placed on the market, FCC equipment authorization rules or other regulations pertaining to consumer devices being placed on the market for use by the general public.

4.1 Anti-Static Handling Procedures

The SOM610 Hardware Development Kit has exposed electronics and chipsets. Proper anti-static precautions should be employed when handling the kit, including but not limited to:

- Using a grounded anti-static mat
- Using a grounded wrist and/or foot strap

4.2 SOM610 DVK Hardware Specifications

4.2.1 SOM610 Block Diagram & specifications

The Processor board provides the basic common set of features with minimal integration efforts for end users. It contains the following:

- QCS610 Main Processor
- Memory : eMMC and LPDDR4x
- PMIC : PM6150 + PM6150L
- SMB1390 Parallel charger
- WCN3980 Atheros Wi-Fi + BT + FM combo chip over SLIMbus, Analog IQ, UART

SOM610 has 40x57 mm² dimension with 3 connectors.

The functional Block diagram is shown in Fig. 4-1.

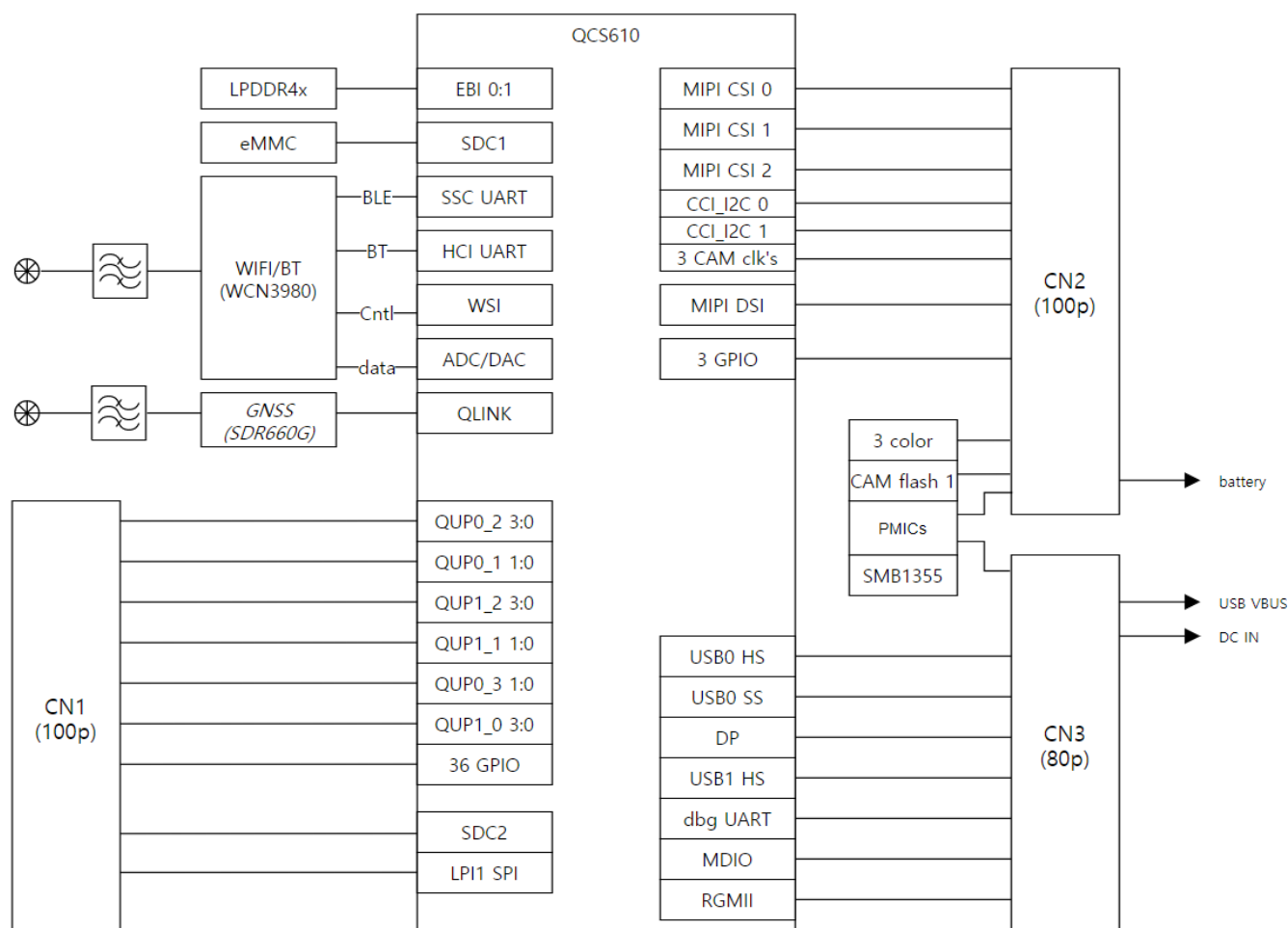


Fig. 4-1 Abstract functional block diagram of SOM610

The specifications of SOM610 are summarized in Table 4-1 below.

Table 4-1 SOM610 specifications

SOM610	
Processors	Qualcomm® QCS610 Octacore 64 bit Kryo 460 CPU Customized, 64-bit ARM v-8 2x 2.2GHz Kryo Gold cores, 6x 1.8GHz Kryo Silver cores Qualcomm® Hexagon™ DSP with dual Qualcomm® Hexagon™ Vector eXtensions (HVX), 1.1 GHz
Memory/Storage	1804MHz LPDDR4x 4GB / eMMC V5.1 64GB
Wireless	Qualcomm® Wi-Fi 802.11a/b/g/n/ac 2.4/5Ghz (WCN3980) with u.FL antenna connector Bluetooth 5.x + BLE

Video	Encode: 5 4K30 8-bit HEVC Decode: 5 4K30 10-bit HEVC/VP9
Graphics	Adreno 608, 3D graphics accelerator with 64-bit addressing, 845 MHz (max freq.) OpenGL ES 3.2, Vulkan, DX 12FL9.3 OpenCL 2.0
Power Management	Qualcomm® Power and battery management (PM6150 + PM6150L + SMB1390)
Display	1 MIPI DSI 4Lane Ports and Touch
Camera	Three 4-lane MIPI CSI 24MP/30fps with dual ISPs, Each ISP capable of 16MP
Ethernet	RGMII
Connectors	100 pin connector x 2 and 80 pin connector x 1 (Panasonic AXK6F00337YG x 3)
AI support	TensorFlow™
Size	40x57

4.2.2 SOM610 DVK Hardware Block Diagram & Specifications

SOM610 DVK specifications use SOM610 specifications as they are, and DVK is summarized in Table 4-2 below to support this.

Table 4-2 SOM610 DVK Specifications

SOM610 DVK	
Audio In / Out	Digital Max 48KHz Sampling rate I2S format, Stereo In-Out Analog Class D type Stereo Speaker Output max 0.6W 8ohm Stereo Headphone Amp Output max 25mW 32ohm / Pop Noise Free at P-On/Off Stereo Line Output (selectable Full-differential / Single-ended) Mono Mic Input
Display	HDMI (mipi-to-HDMI) Pin header for DP (Expansion board for DP)
Camera	Pin header for 3 MIPI CSI (Expansion board for MIPI CSI)
USB-C Jack	USB Type C with VESA DisplayPort V1.3 support
Storage Expansion	MicroSD card socket
GPIO / QUP	Pin Headers for GPIO and QUP
Buttons	3 Tact Switch buttons
WIFI/BT Antenna Port	1 WIFI/BT antenna SMA Connectors
Ethernet	1Gb Ethernet, RJ45
Debug	Debug UART to RS-232 RJ-9 Connectors
LED	3 Color Debug LEDs
Size	TBD
Power Jack Support	5V@3A adaptor included

SOM610 DVK block diagram is shown in Fig. 4-2. Please refer to the circuit diagram for details.

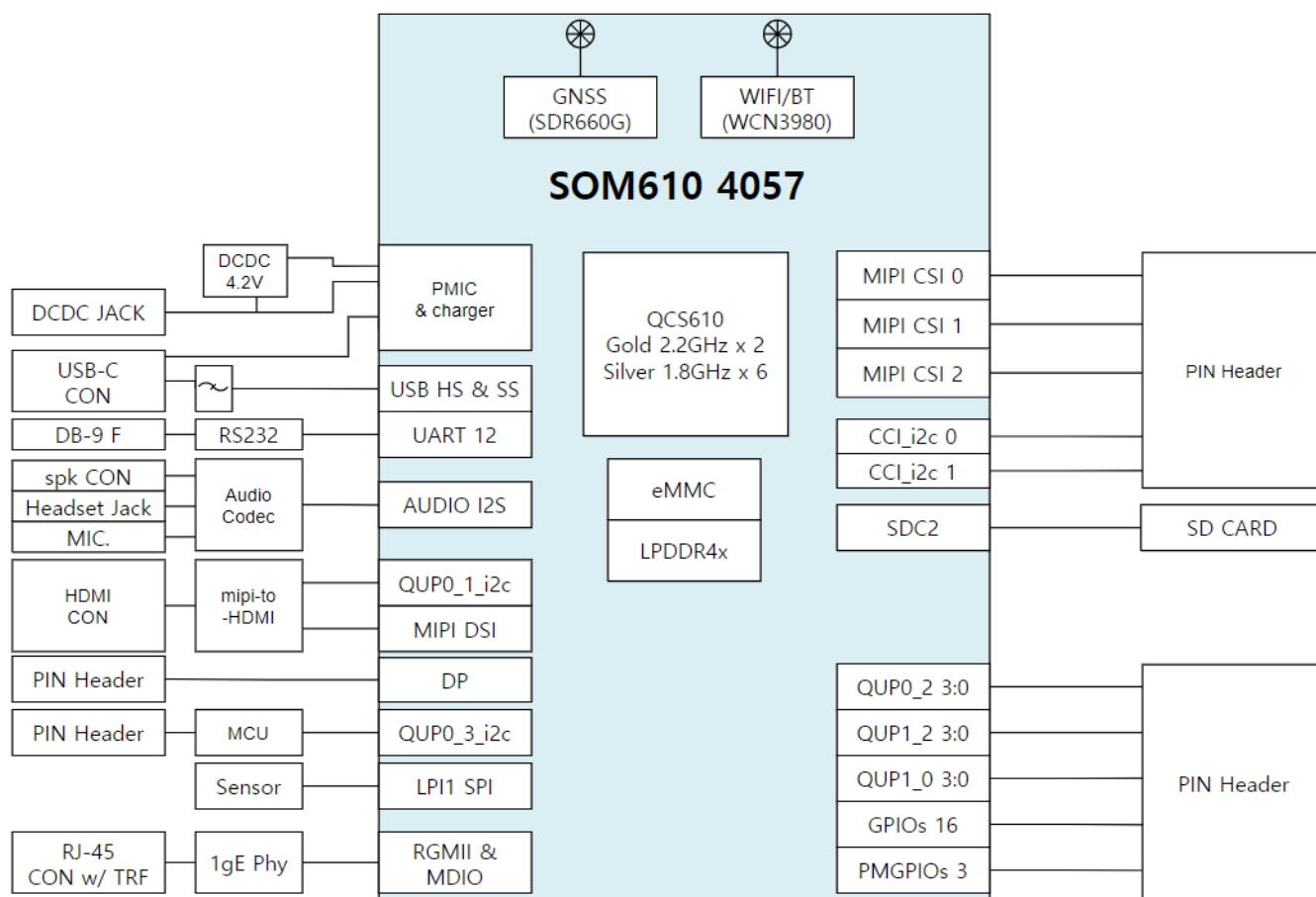


Fig. 4-2 SOM610 DVK block diagram

4.3 SOM610 DVK Hardware Port Description

SOM610 DVK carrier board is equipped with SOM610 module. To operate this board, a power adapter must be inserted, and a jumper terminal block must be inserted for several settings.

This section describes I/O ports for using the carrier board. The outline diagram of DVK is as Fig. 4-3 below.

SOM610 DVK Carrier board is stacked with SOM610 and several extension modules. And to operate this, the DVK requires power adaptors and several board jumper terminal blocks.

This section describes the DVK's I/O ports and the usage of the DVK. The DVK picture is Fig. 4-3 below :

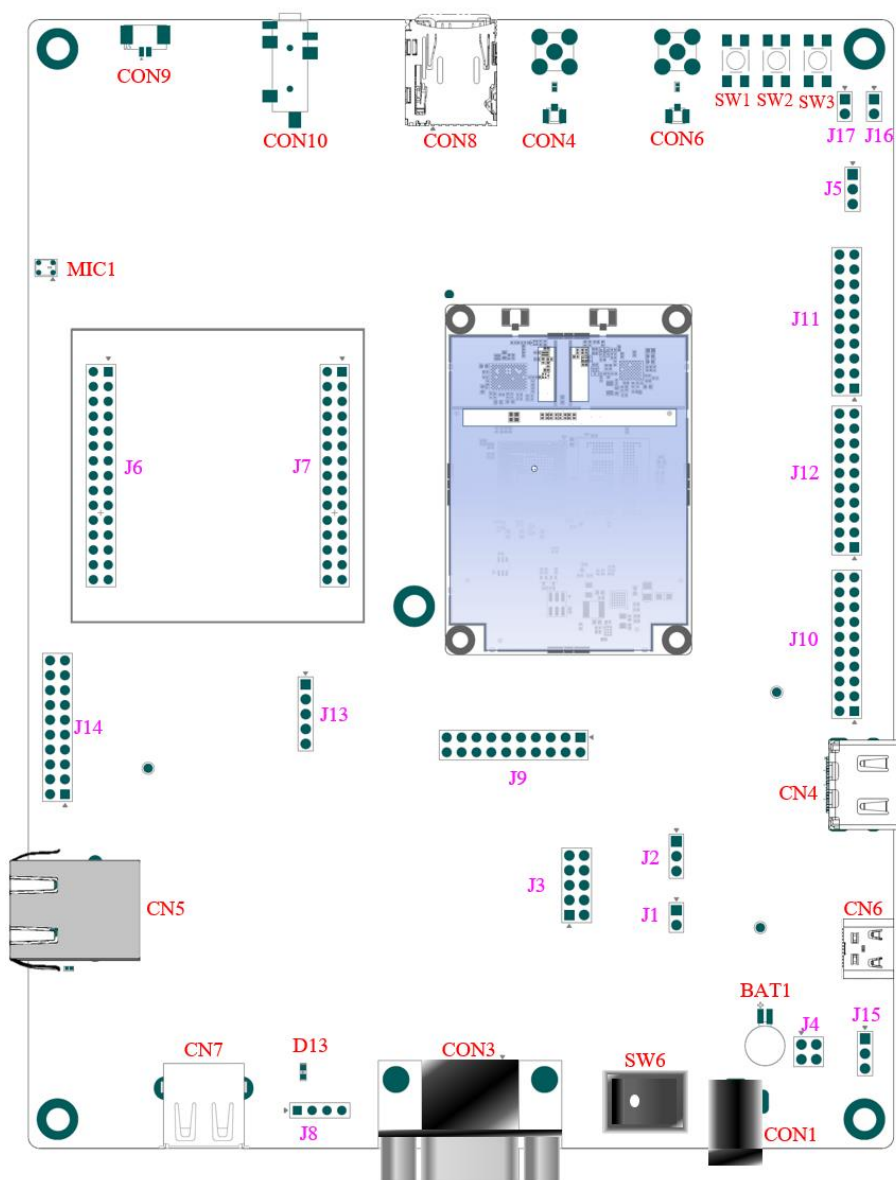


Fig. 4-3 Outline Diagram of SOM610 DVK V1.1

The names of I/O ports and their descriptions in Fig. 4-3 are summarized in Table 4-3 below. This section describes the ports in the numerical order shown in Fig. 4-3.

Table 4-3 Connector Ports Names on Fig. 4-3

No.	Name	Section	Ref. # of Fig4-3
1	USB A CONNECTOR, CN7	4.3.1	CN7
2	Debug UART PIN Header, J8 (NOT implemented)	4.3.2	J8
3	RS-232 Debug Connector, CON3	4.3.3	CON3
4	Power On/Off Toggle Switch, SW6	4.3.4	SW6
5	DC Power Input Adaptor Jack, CON1	4.3.5	CON1
6	Boot Option Pin Header, J4	4.3.6	J4
7	USB_CC1 Jumper Pin Header, J15	4.3.7	J15
8	USB-C connector, CN6	4.3.8	CN6
9	HDMI Output Connector, CN4	4.3.9	CN4
10	MIPI CSI Camera PIN Headers, J10, J12 and J11	4.3.10	J10, J12, J11
11	3 Color LED PIN Header, J5 (NOT implemented)	4.3.11	J5
12	Home Key and H/W Reset Pin Headers, J16, J17 (NOT implemented)	4.3.12	J16, J17
13	Key Button Tact Switches, SW1, SW2, SW3	4.3.13	SW3, SW2, SW1
14	Antenna Connectors, CON4 ~ CON7	4.3.14	CON4~CON7
15	Micro SD Card slot, CON8	4.3.15	CON8
16	Analog Headset Output Phone Jack, CON10	4.3.16	CON10
17	Analog Speaker Output Connector, CON9	4.3.17	CON9
18	Analog Microphone, MIC1	4.3.18	MIC1
19	GPIO Pin Headers, J6, J7	4.3.19	J6, J7
20	Microprocessor GPIOs PIN Header, J14	4.3.20	J14
21	Microprocessor F/W download PIN Header, J13 (Not Implemented)	4.3.21	J13
22	DP Output PIN Header, J9	4.3.22	J9
23	Ethernet RJ45 Connector, CN5	4.3.23	CN5
24	DVK Main Power Selection Jumper PIN Header, J3	4.3.24	J3
25	Battery Power PIN Header, J2 (Not Implemented)	4.3.25	J2
26	DC to Battery Power Jumper PIN Header, J1	4.3.26	J1
27	Summary : Default Board Jumper Setting, J1, J3, J4, J5	4.3.27	J1,J3,J4,J15

4.3.1 USB A CONNECTOR, CN7

The CN7 connector is a USB A connector and is connected to the QCS610's USB1 high speed data port. This port is a separate USB port from the USB0 port and supports the USB host function. USB_VBUS power output to this connector is available only when GP41 is turned on.

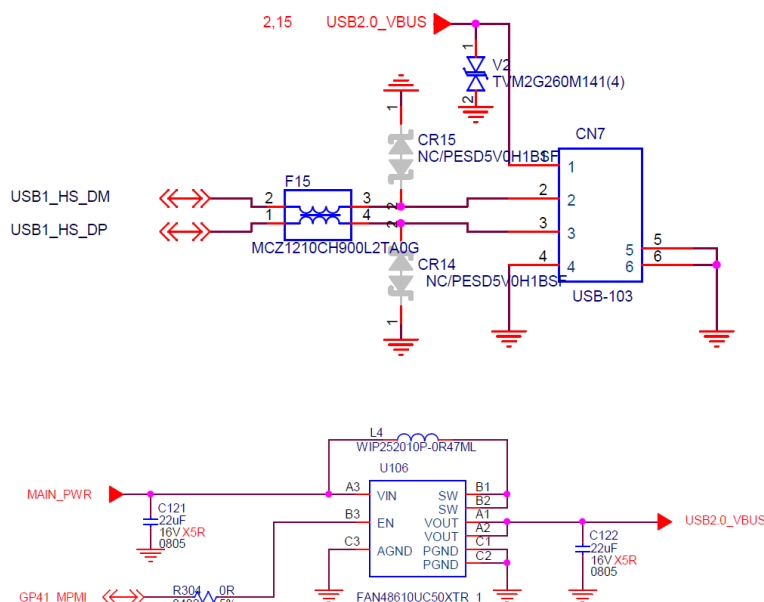


Fig. 4-4 Circuits about CN7

4.3.2 Debug UART PIN Header, J8 (NOT implemented)

There is J8 for UART debugging, but the corresponding PIN header is not actually assembled in SOM610 DVK.

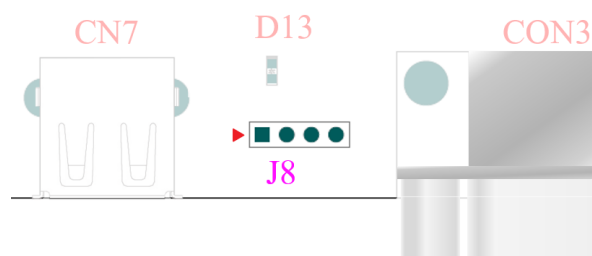


Fig. 4-5 Location of J8

Pin 1 of J8 is where there is a red triangle on the left of J8 in Fig. 4-5, and the pin number sequentially increases in the right direction. The related circuit is shown in Fig. 4-6. The voltage level of the signal is 1.8V, the default voltage level of pin 1 is 3.3V, and it can be 3.13V depending on the board revision. Signals are susceptible to ESD and should be handled carefully. We are not responsible for ESD failure caused by user negligence.

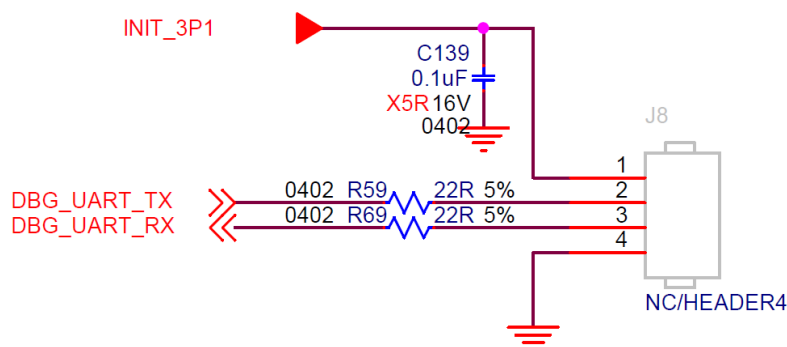


Fig. 4-6 Circuits about J8

4.3.3 RS-232 Debug Connector, CON3

SOM610 DVK is prepared with a standard DSUB-9 female connector for RS-232 input/output, allowing RS-232 communication with a PC. As a port for debug monitor, it can receive serial monitoring messages from the bootloader during booting from the PC, and can operate as a console of the system if necessary. The circuit is as follows. QUP0_0, which is QCS610 debug UART, is used and LPI debug UART is basically not supported.

It provides the debug serial UART port for debugging the system, which is converted to RS232 to enable communication with the PC via CON3, the DB-9 Female connector. The circuit is shown in the Fig. 4-7 below and refer to the circuit provided for more details.

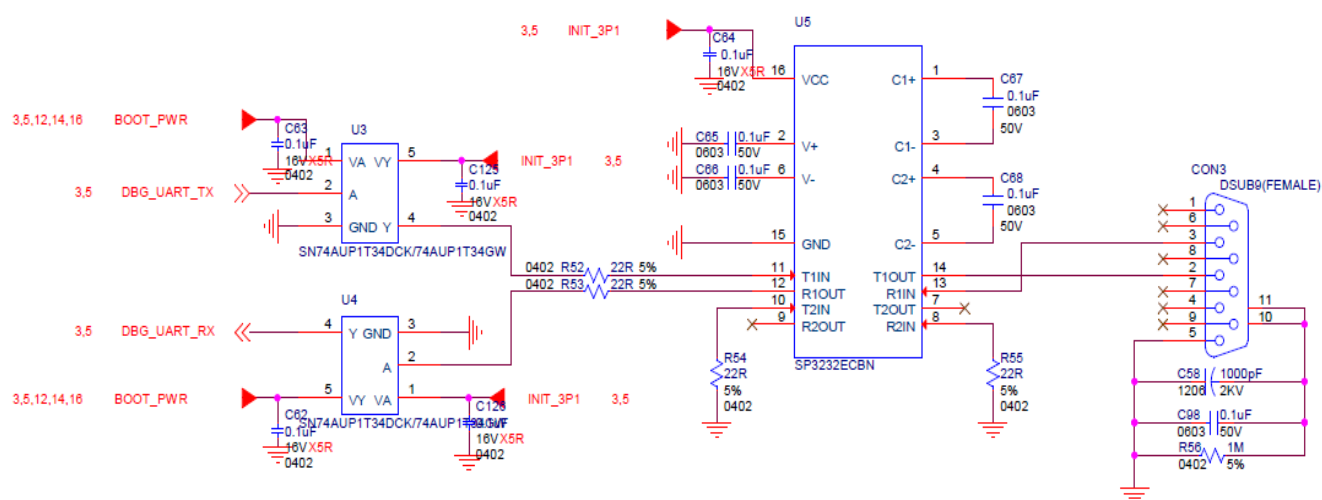


Fig. 4-7 Debug Serial RS232, DB-9 F Connector

4.3.4 Power On/Off Toggle Switch, SW6

When power is permitted to the DC adapter jack(4.3.4) and the Power On/Off toggle switch SW6 is set to On, power is applied to the board. Since there is no surge protection circuit or noise reduction circuit in relation to the input power, you must leave SW6 Off before plugging in the adapter to protect the DVK internal circuit. The circuit related to SW6 is as Fig. 4-8 below.

The DC adaptor plug can be connected to the jack on the board (⑤,section 4.3.5), and the SW6 Power On/Off switch is turned on to supply power to the system.

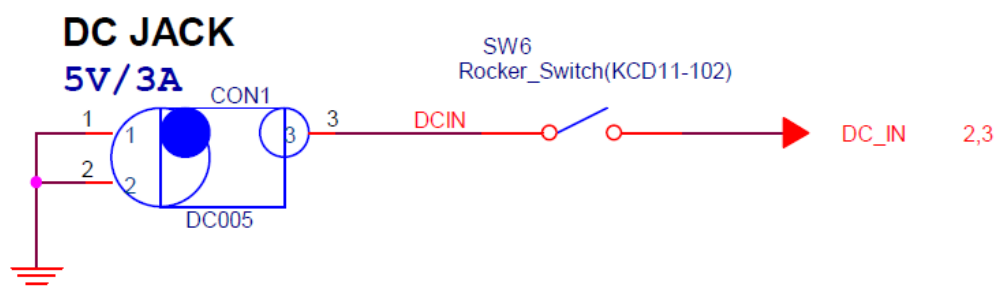


Fig. 4-8 SW6 circuits of SOM610 DVK Carrier board

DC_IN output by turning on SW6 becomes the source of the next power.

- 1) Main DC power of SOM610
- 2) Main power used by DVK Carrier board
- 3) Power to make V_BATT

3) will be explained in detail in 4.3.25 and 4.3.26, and the contents against 1) and 2) will be explained in 4.3.4.1 and 4.3.4.2.

4.3.4.1 Main DC power of SOM610, DC_IN

DC_IN of CON3 is a power supply for SOM610 that is different from USB_VBUS_CONN mentioned in section 4.3.8.1. USB_VBUS power can be input or output according to the USB power role, but DC_IN is only the input power for SOM610. According to the specifications, it can be up to 12V. DC_IN supplied from SW6 is connected to pins 1, 3, 5, 7 and 9 of CON3.

DC_IN power alone is not enough to operate the SOM610 and requires battery power. However, the SOM610 can be operated by supplying battery power from an external power source without a battery. It can be made with a DC_IN power, which will be described in section 4.3.25.

4.3.4.2 Main power used by DVK Carrier board, MAIN_PWR_SRC

MAIN_PWR_SRC is the power used inside the DVK Carrier board. Because the voltage of DC_IN can be up to 12V, it cannot be used as an input power such as a LDO of DVK Carrier board, so the voltage of DC_IN is lowered to 4.53V with a DC-DC converter to make it one of the system power source. The related circuit is shown in Fig. 4-9.

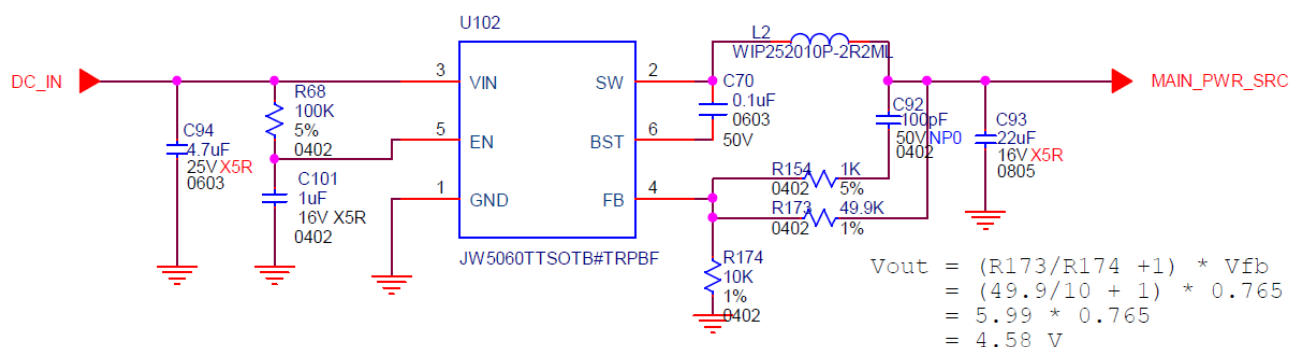


Fig. 4-9 Generation of MAIN_PWR_SRC from DC_IN

MAIN_PWR_SRC is one of the main power sources of the DVK Carrier board, and the main power source is determined by J3. For J3, see section 4.3.24.

4.3.5 DC Power Input Adaptor Jack, CON1

The electrical input standard allowed for this DVK must follow the contents described in 3.4 and 3.5, which means that adapter standard provided with DVK is a product within 5V@3A DC power supply above. If power is supplied to the DC adapter jack using a product or standard other than the supplied adapter, please use it according to the conditions described above to prevent failure.

The power jack connector of Fig. 4-8 circuit used for SOM610 DVK is shown as Fig. 4-10 below. Please use the appropriate adapter standard.

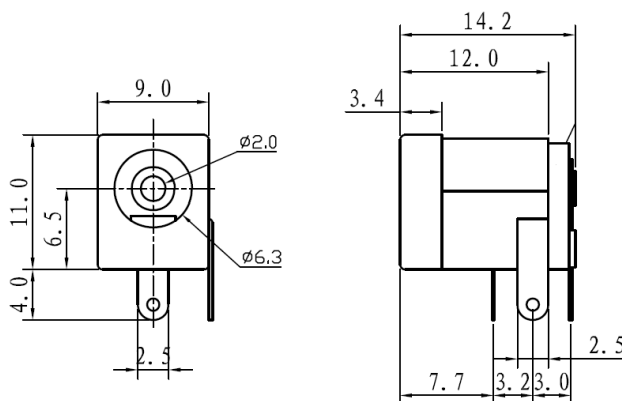


Fig. 4-10 Adaptor Jack Mechanical Drawing

4.3.6 Boot Option Pin Header, J4

There are two boot options, one is USB boot and the other is micro-SD card boot.

All boot options must be set before power on.

For USB boot option, jumper setting is done as shown in Fig. 4-11. When the power is turned on, the SOM610 enters USB forced boot mode. The USB boot option is used when fusing the OS again using QFIL. How to use QFIL is not covered here.

Currently, micro-SD card boot option is not supported, so do not connect Pin 1 and Pin 2 of J4.

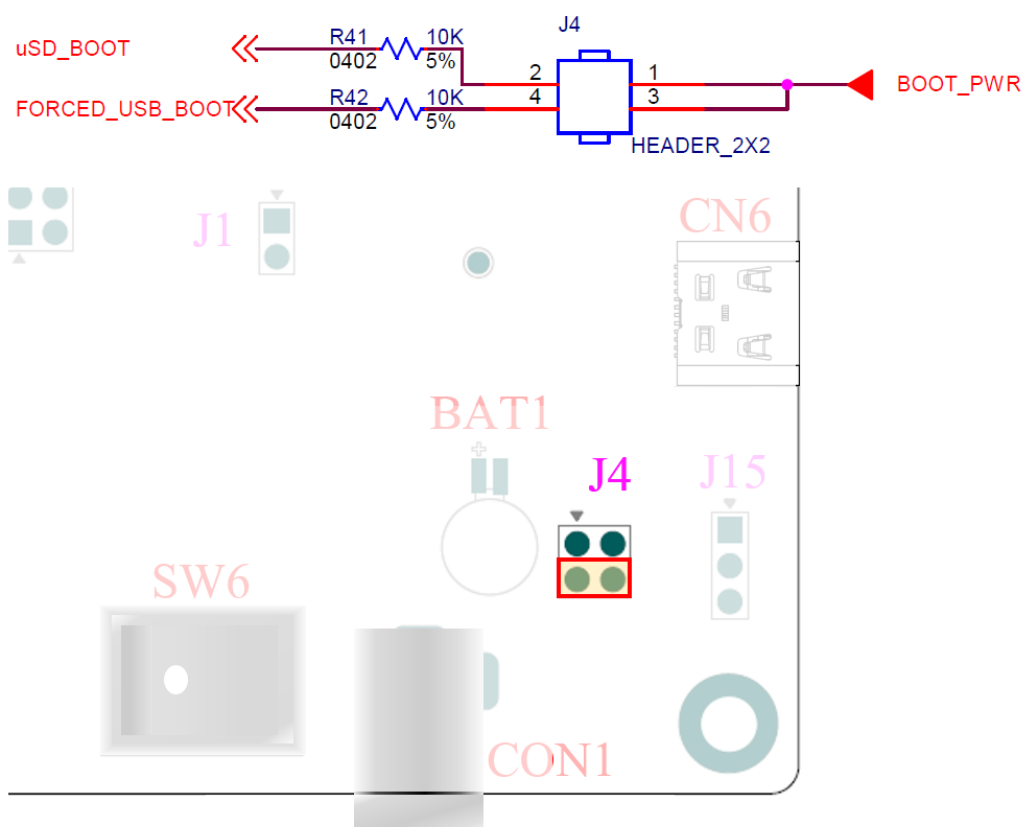


Fig. 4-11 Set FORCED_USB_BOOT

4.3.7 USB_CC1 Jumper Pin Header, J15

Fig. 4-12 shows the default jumper setting that connect Pin 1 and Pin 2 of J15.

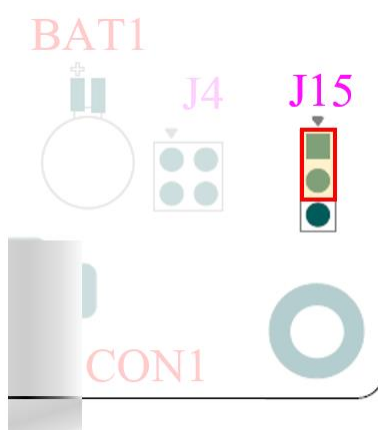


Fig. 4-12 Default position of Jumper for J15

The default jumper setting is the setting that directly connects USB_CC1 of SOM610 and USB3_CC1_CONN of USB-C connector as shown in Fig. 4-13

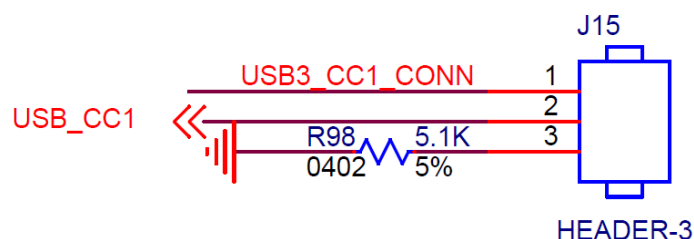


Fig. 4-13 USB_CC1 selection for J15

If you want to connect a device to the USB-C connector or change the power role such as DFP / UFP, It is also possible to test by inserting a circuit such as User Defined Pullup / Pulldown of the function corresponding to J15. Please note that pin 2 of each header pin is a signal that goes inside SOM610.

Unlike USB_CC1, USB_CC2 is directly connected between the USB-C connector and SOM610 as shown in Fig. 4-14.

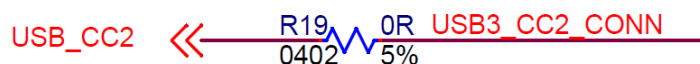


Fig. 4-14 Circuits for USB_CC2 signal

For detailed information about the related USB_CC and corresponding USB functions, it is not covered in this document. Please refer to Qualcomm's document number below. We do not have the right to distribute

the applicable Qualcomm documents, and please obtain them separately in compliance with Qualcomm's licensing policy.

Qualcomm Document Number : 80-PH856-5A PM6150/PM6250/PM7150 Power Management IC Design Guidelines and Training Slides

4.3.8 USB-C Connector, CN6

The location of CN6, the USB-C connector, is shown in Fig. 4-15

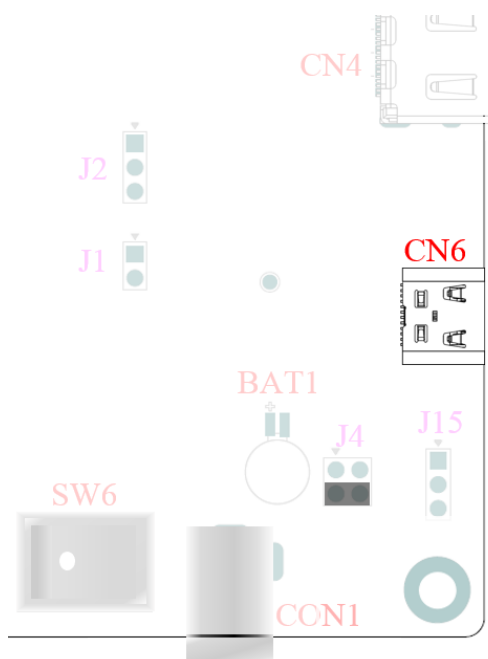


Fig. 4-15 Location of USB-C connector CN6

The USB-C connector of SOM610 DVK provides the following functions.

- USB-VBUS
- USB 2.0 / 3.0 data communication

One of the most important features of SOM610 DVK is related to the USB-C power function. This is described in the section below.

The circuit connection of the USB-C connector is shown in Fig. 4-16.

Regarding the power function, signals of USB_CC1 and USB_CC2 are supported, and these signals are described in section 4.3.7.

The USB-C connector allows the use of the USB-VBUS power, USB 2.0/3.0 data line, and display port.

It cannot boot with a USB-C only power configuration that connects to the PC, and requires an auxiliary power source. The auxiliary power sources are described in section 4.3.5 and/or 4.3.25. However, if the

disconnected.

If the default jumper setting of USB_CC1 mentioned in section 4.3.7 is changed, the SOM610 DVK cannot be connected to the PC because the role of SOM610 has been changed to the USB Host.

4.3.9 HDMI Output Connector, CN4

The primary display supported by SOM610 DVK is HDMI. The location of HDMI connector is shown in Fig. 4-17.

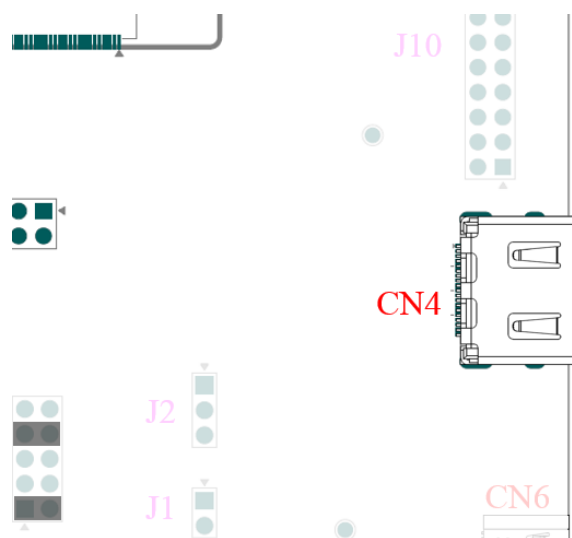


Fig. 4-17 Location of HDMI connector

SOM610 DVK converts MIPI-DSI signal to HDMI signal and sends it to HDMI connector. Audio output through the HDMI connector is not supported.

To support audio output, HW and SW modifications are required, so a separate inquiry is required.

4.3.10 MIPI CSI Camera PIN Headers, J10, J12, J11

The SOM610 DVK provides 3 pin headers for MIPI-CSI to support camera connection. The number of each connector is J10, J12, J11. Note that each connector has a different pin arrangement and number. Fig. 4-18 shows that the pin header spacing of each connector is different. Therefore, please refer to the DXF file of the SOM610 DVK Carrier board mentioned in section 2.1 for more accurate arrangement.

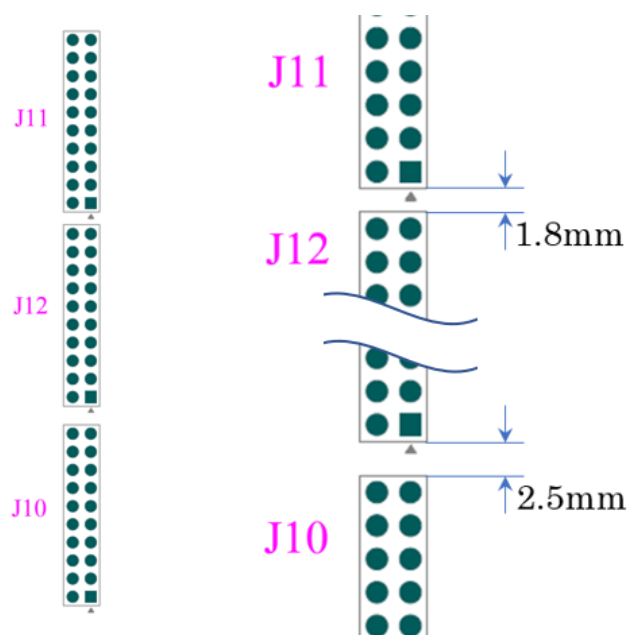


Fig. 4-18 Positions for MIPI CSI's

4.3.10.1 J10 for MIPI CSI#0

J10 is allocated to support the camera port MIPI CSI #0 on the carrier board. The circuit for this is shown in Fig. 4-19, and the pin position, orientation and order of pins is shown in Fig. 4-20.

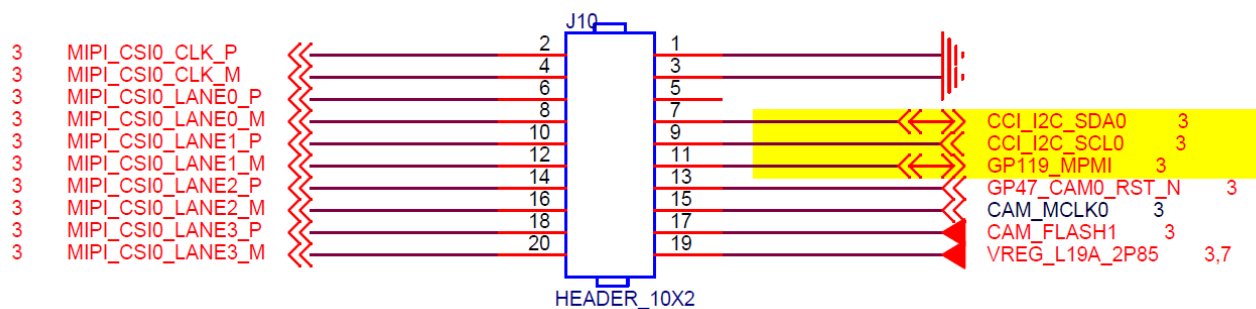


Fig. 4-19 Pins of Camera CSI#0 Pin Header, J10

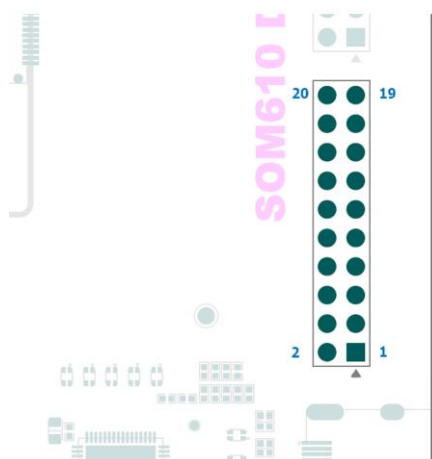


Fig. 4-20 Pin position and orientation for J10

4.3.10.2 J12 for MIPI CSI #2

The pin header circuit of MIPI CSI #2 is shown in Fig. 4-21. Only cameras with ISP can connect to MIPI CSI #2.

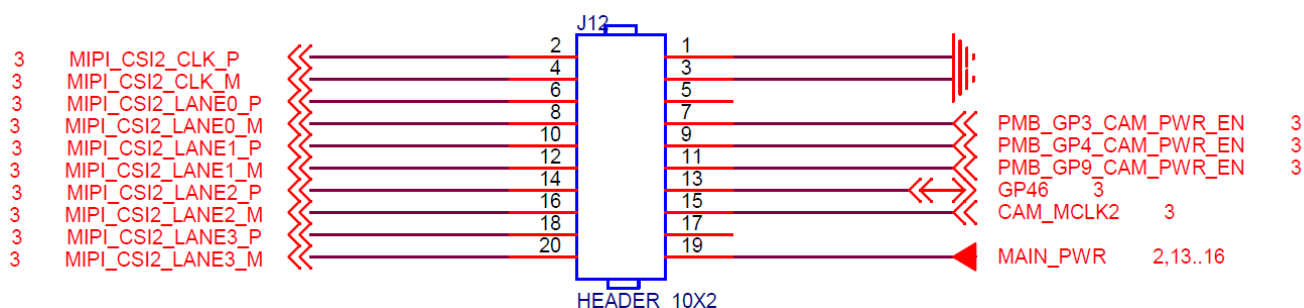


Fig. 4-21 Pins of Camera CSI #2 Pin Header, J12

The pin position and orientation of J12 is shown in Fig. 4-22.

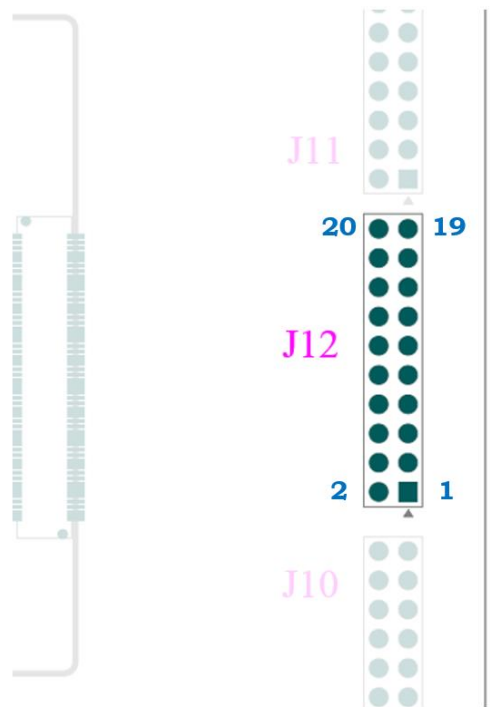


Fig. 4-22 Pin position and orientation for J12

4.3.10.3 J11 for MIPI CSI #1

J11 is allocated to support the camera port MIPI CSI #1 on the carrier board. The circuit for this is as Fig. 4-23, and the pin position, orientation and order of pins is shown in Fig. 4-24.

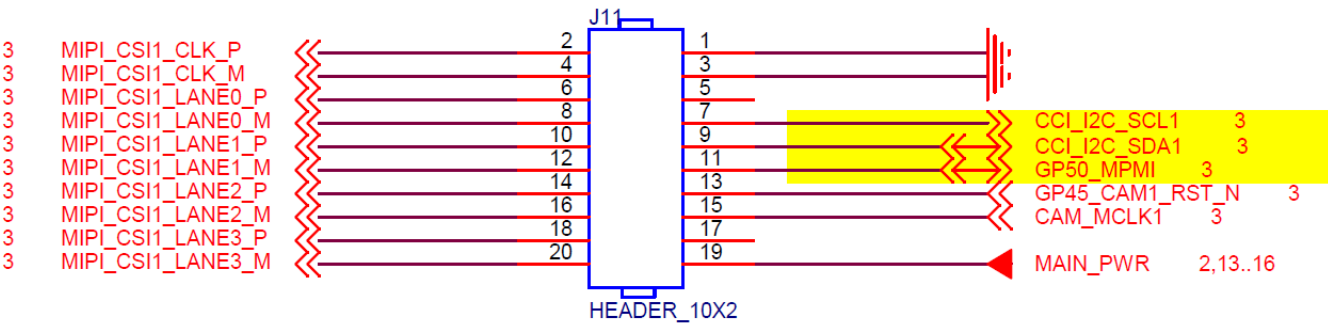


Fig. 4-23 Pins of Camera CSI #1 Pin Header, J11

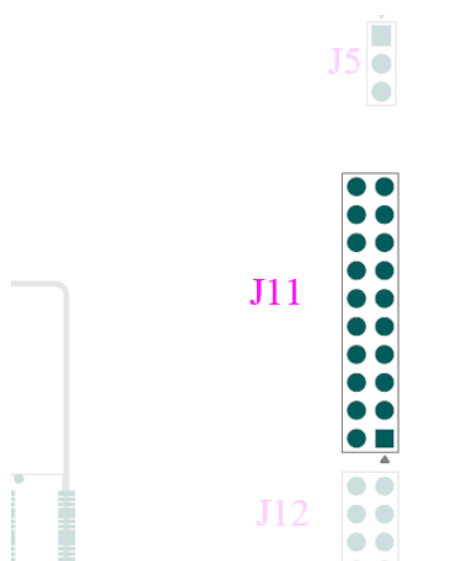


Fig. 4-24 Pin position and orientation for J11

4.3.11 3- Color LED PIN Header, J5 (NOT implemented)

SOM610 DVK supports J5 to check the signal of the internal three color LED. The location of J5 is shown in Fig. 4-25.

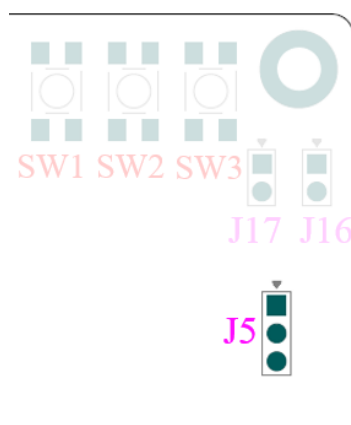


Fig. 4-25 Location for J5

The pin header for J5 is not mounted as a default, and J5 is a test point to check the signal. The signals of J5 are the signals of PM6150 inside SOM610 and are displayed based on the scenario in Android system. The three color LEDs connected to J5 are on SOM610 DVK and the circuit is shown in Fig. 4-26.

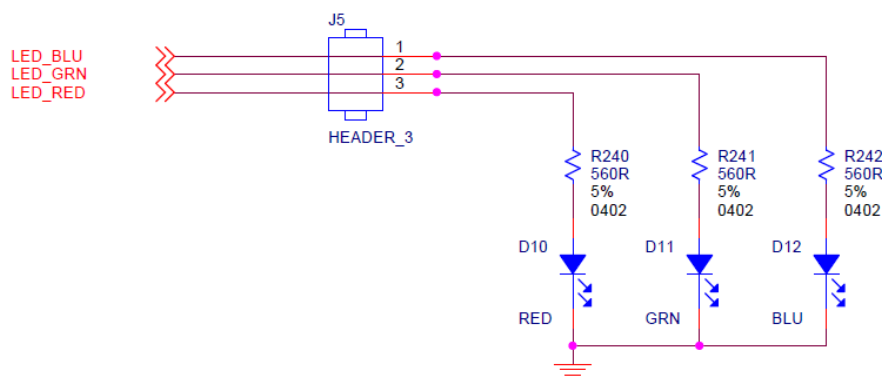


Fig. 4-26 Pins for J5

4.3.12 Home Key and H/W Reset Pin Headers, J16, J17 (NOT implemented)

Home key is not currently used in Android. Even if a switch for Home key is attached, the actual function differs depending on Android version, so it is supported as a test point. Related to Home key function, you can test it using the corresponding test point.

Since HW Reset function is supported from SOM610 v1.1, there is no switch for HW reset and it is supported as a test point. HW Reset doesn't work properly in SOM610 v1.0 or earlier, so don't use it. The circuit for Home key and HW Reset is shown in Fig. 4-27.

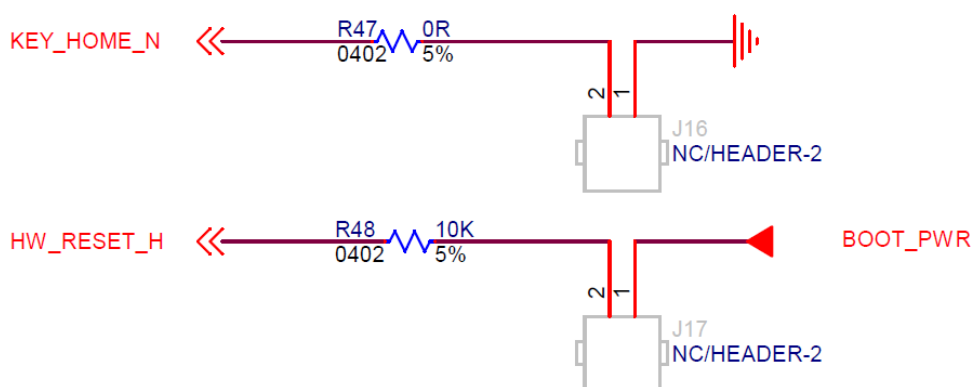


Fig. 4-27 Pin Headers of Key Home & HW Reset

HW Reset button physically forces to reset SOM610 module regardless of the S/W function.

This function is a necessary function for development, which is used when you want to update quickly or when you want to force the reset and the S/W system cannot be reset for some reason.

The signal of this button directly resets PMIC inside SOM610.

Therefore, if you press this button at any moment, normally the system reboots immediately from the current working state in any situation of the S/W.

It operates regardless of S/W, which is not guaranteed to save the current work. Keep this button pressed for 0.1 second and release the button, and then a reset is activated at that time. This button switch is used to physically reset the system. Press and release for at least 0.1sec, and the system resets and reboots.

4.3.13 Key Button Tact Switches, SW1, SW2, SW3

There are 3 Tact Switch buttons on the carrier board of SOM610 DVK, and they are in charge of a unique function that is not user-defined. The location of Tact Switch is shown in Fig. 4-28, the related circuit is shown in Fig. 4-29.

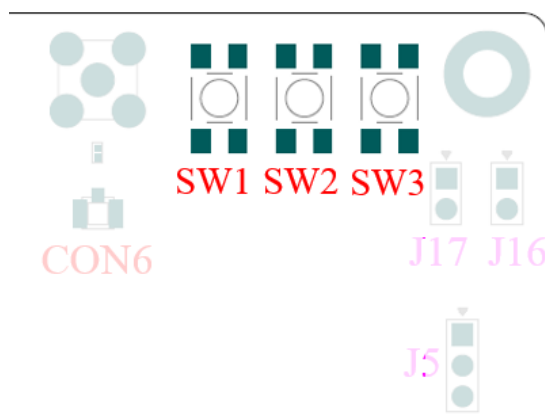


Fig. 4-28 Locations of SW1, SW2 and SW3

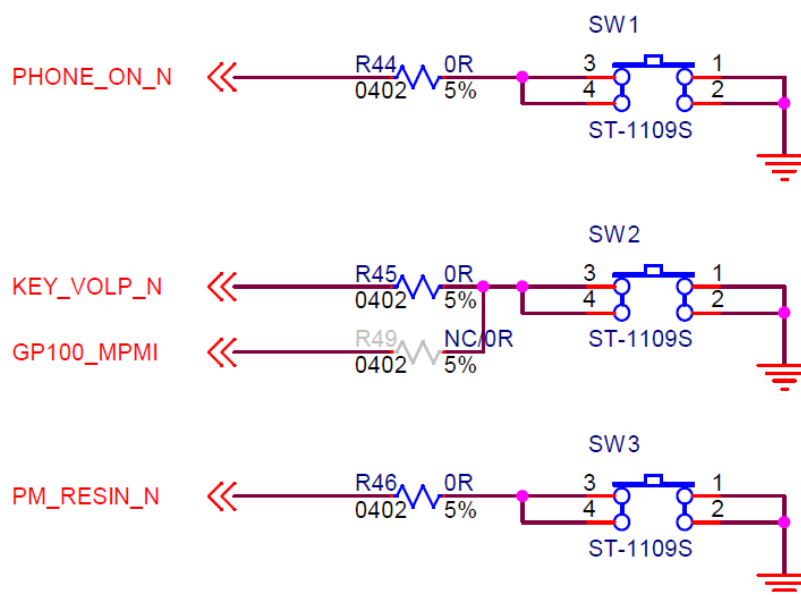


Fig. 4-29 Signals for SW1, SW2 and SW3

4.3.13.1 S/W Power, SW1

This signal is input as KPD_PWR_N signal of PM6150, PMIC of SOM610. When there is only VBATT+ power without USB_VBUS_CONN power on the DVK carrier board, press this button to turn on the system and start booting.

When this button is pressed while booting into the OS, it can be interpreted in S/W as a sleep/wakeup signal. In addition, if you press it for a long time longer than a few seconds or press it with a key button combination other than SW1, other functions can be operated, and all operations related to this are defined in S/W.

The input signal of this button is entered as the Phone ON pin of PM6150 which is the PMIC of the SOM610 and performs the function of the power button while the power is applied. Pressing this button with the first VBATT+ generated will cause the system to boot. For example, if the Android system is booted, a light push & release of the button will cause the system to toggle between the WAIT and the SUSPEND status, not the POWER ON and POWER OFF.

4.3.13.2 Volume Up, SW2

The signal of Volume Up is input to the GPIO_02 signal of the PM6150L in the SOM610 module. This button signal is mapped to the audio volume up function, but other functions are defined in S/W.

The input signal of this button is entered as the Volume Up pin of PM6150 which is the PMIC of the SOM610.

4.3.13.3 Volume Down, SW3

The signal of Volume Down is input to RES IN of PM6150. This button signal works as an audio volume down function while Android is running, but also performs other functions of Android system in combination with other buttons.

4.3.14 Antenna Connectors, CON4 ~ CON7

The WIFI/BT antenna of SOM610 is connected to CON4/CON6 using a u.FL type coaxial cable connector, and then is connected to the SMA antenna through CON5/CON7.

If you connect to CON6(or CON4) with an RF cable from the RF connector terminal of SOM610 (Fig. 3-7), you can equip CON7(or CON5) with SMA antenna. The circuits of CON6 are same as Fig. 4-30.

The antenna connected to the SMA connector is subordinate to the function and performance of the port supported by SOM610. Please refer to section 3.6.4 about this.

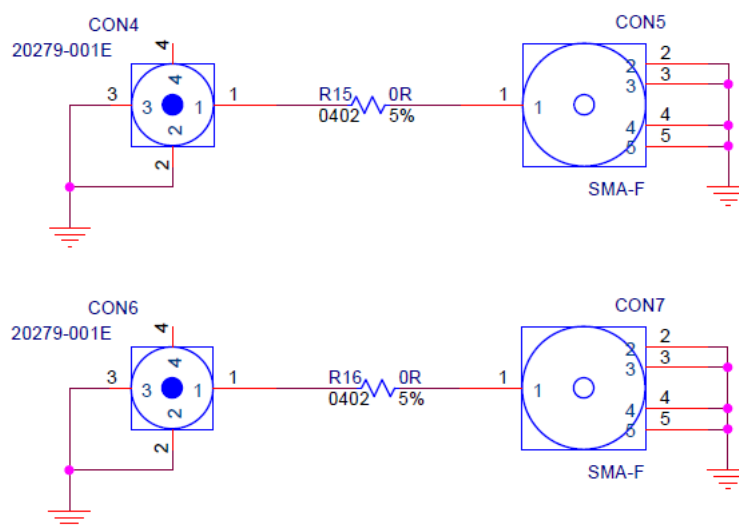


Fig. 4-30 WIFI/BT SMA Connector

4.3.15 Micro SD Card Slot, CON8

There is a card connector CON8 on the top of the DVK to support Micro-SD external memory cards.

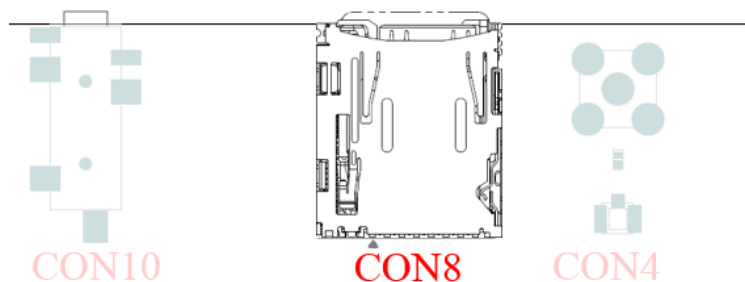


Fig. 4-31 micro-SD Card slot, CON8

Please inquire separately for supported memory capacity.

Booting from Micro-SD card is not yet supported, and will be supported in the future.

4.3.16 Analog Headset Phone Jack Connector, CON10

Audio codec supported by SOM610 DVK is Realtek's ALC5633Q or ALC5640-VB. By default, ALC5633Q is mounted, but it can be changed to ALC5640-VB without any notice depending on chip supply and demand conditions.

The analog headset stereo output signal follows the specifications of the built-in amplifier of the audio codec and is output to the 3.5 pie headset jack, CON10. The circuit of CON10 is shown in Fig. 4-32 and the location of CON10 is shown in Fig. 4-33.

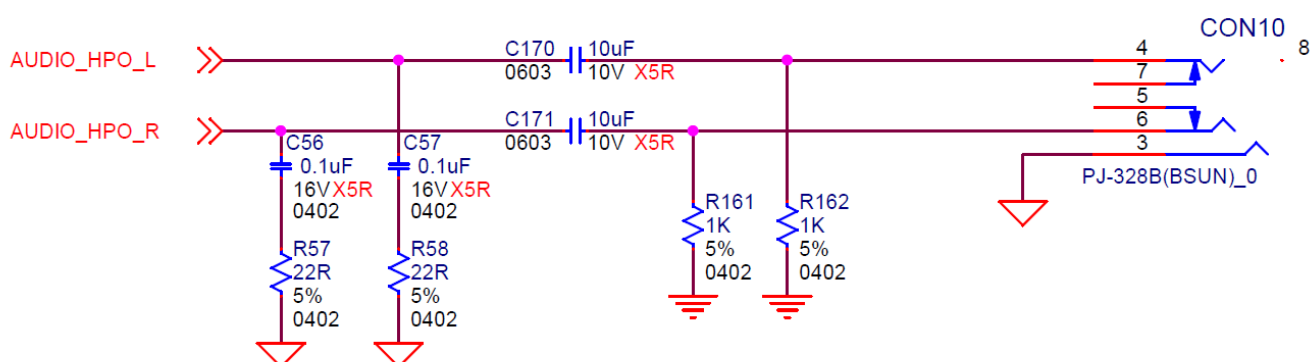


Fig. 4-32 Circuits of Headset Jack, CON10

4.3.17 Analog Speaker Output Connector, CON9

SOM610 DVK supports analog micro speaker output through CON9. The location of CON9 is shown in Fig. 4-33.

Additional testing by the user is required if the environment changes, such as changing the audio codec, wanting a higher output, or changing the analog speakers.

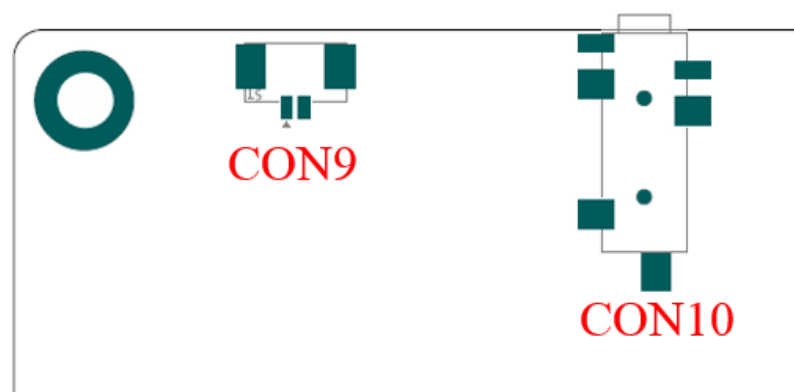


Fig. 4-33 Analog Sound Outputs, CON9 and CON10

The output of the micro speaker depends on the voltage supplied to the speaker amplifier inside the audio codec used in the SOM610 DVK. There are two sources of voltage supplied to the speaker amplifier, please refer to section 4.3.24 for details.

4.3.18 Analog Microphone, MIC1

SOM610 DVK supports analog microphones. The hole for the analog microphone is located at the top, and if foreign substances enter this hole, the performance may deteriorate or malfunction, so please manage it with care. The location of MIC1 is shown in Fig. 4-34.

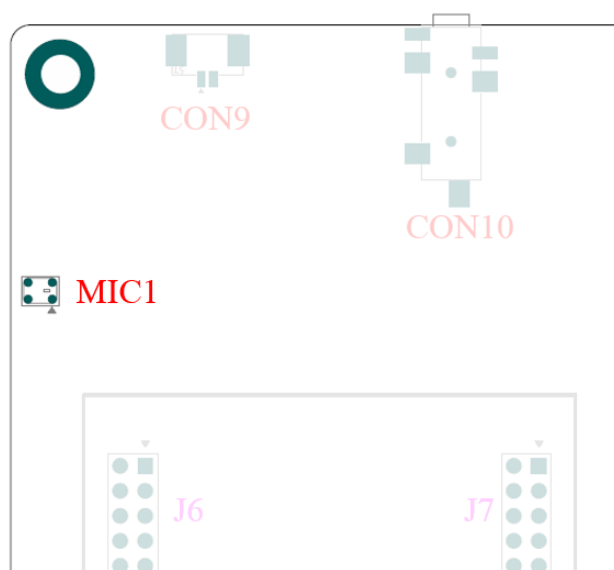


Fig. 4-34 Location of Microphone, MIC1

4.3.19 GPIO Pin Header J6, J7

GPIOs whose purpose is not determined in SOM610 DVK are assigned to J6 and J7, and the signals assigned to J6 and J7 are shown in Fig. 4-35. All general signals except power have 1.8V level and are connected to QCS610 or PMIC. Signals whose names begin with LPI cannot be used for general purpose and must be used for a specific sensor.

Please inquire separately for a list of available sensors.

The location of J6 and J7 is shown as Fig. 4-36. Please refer to the DXF file mentioned in section 2.1 for the information on the gap between J6 and J7.

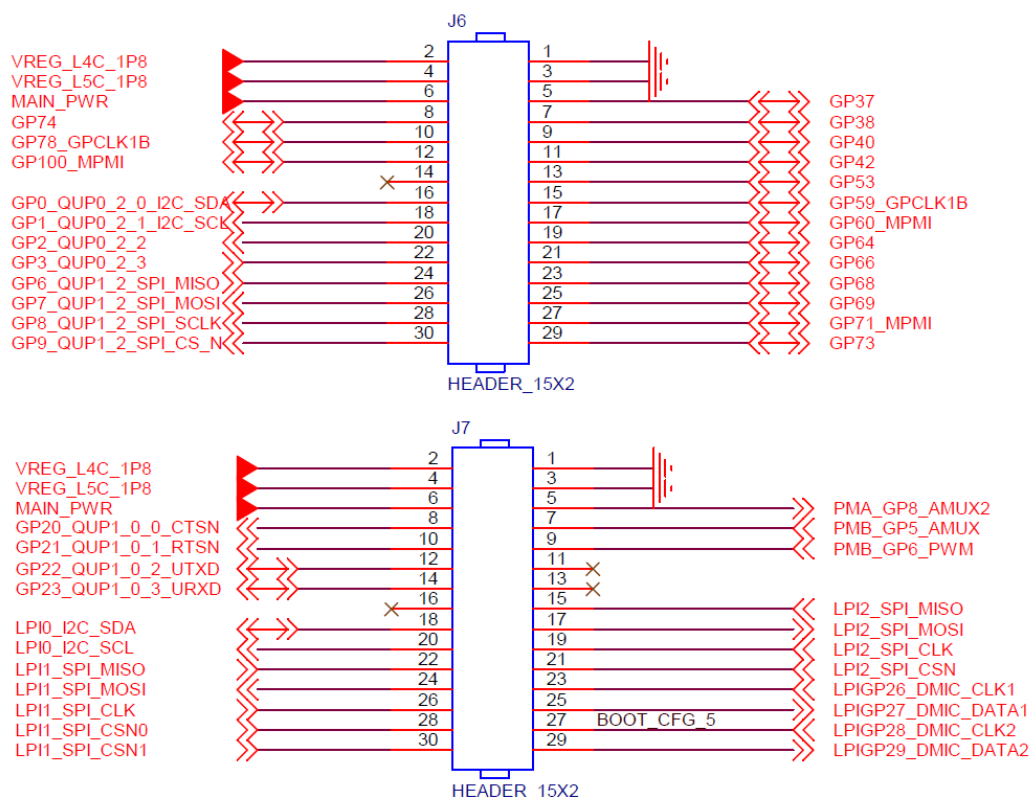


Fig. 4-35 Signals of J6 and J7

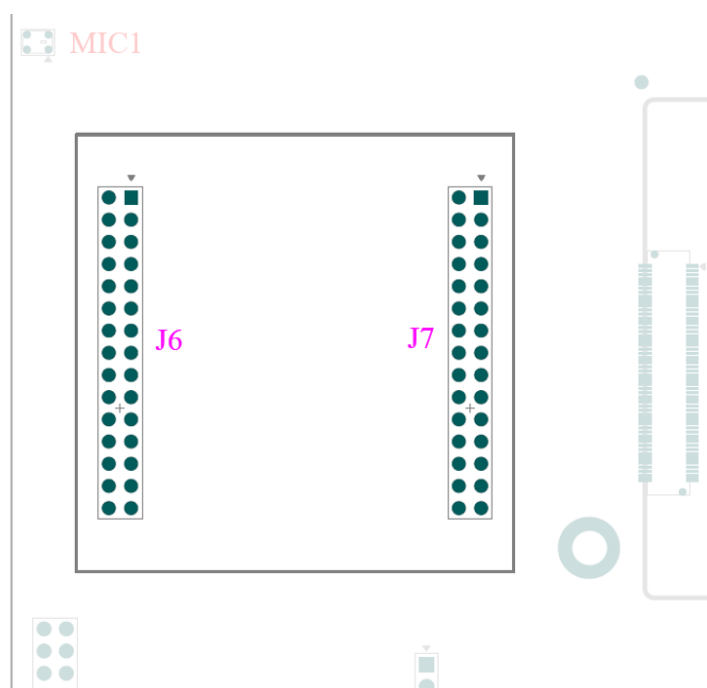


Fig. 4-36 Locations of J6 and J7

4.3.20 Microprocessor GPIOs PIN Header, J14

It is a pin header connector for GPIO expansion that supports functions through the microprocessor in the SOM610 DVK.

This feature has not been implemented yet.

4.3.21 Microprocessor F/W download PIN Header, J13 (Not Implemented)

It is a pin header connector for downloading the F/W of the microprocessor mentioned in section 4.3.20, and it is not mounted by default.

4.3.22 DP Output PIN Header, J9

Signals for display port exist in SOM610 and are assigned to Pin Header J9 as shown in Fig. 4-37. The location of J9 is shown in Fig. 4-38.

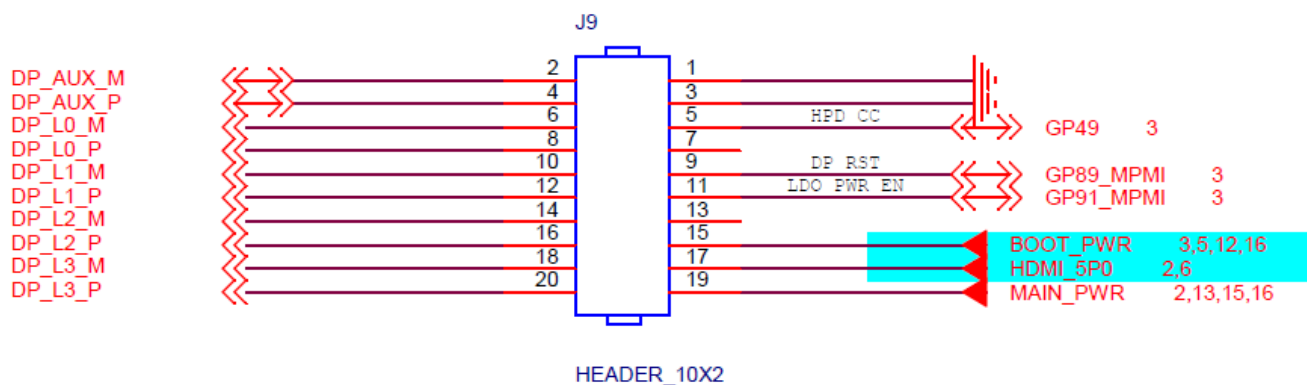


Fig. 4-37 DP Pin Header, J9

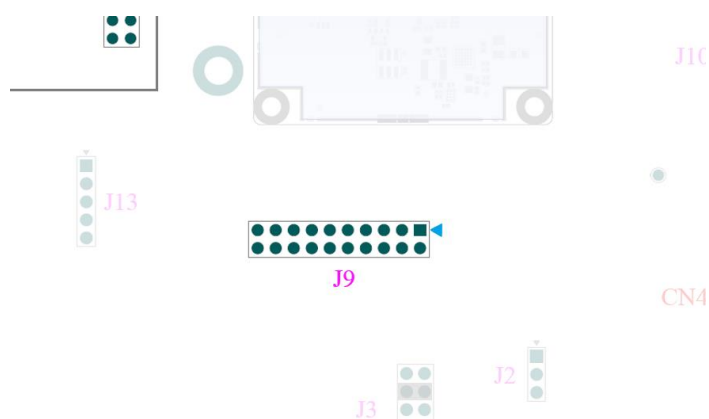


Fig. 4-38 Location of J9

Display port output can be converted to HDMI output through a daughter board that can be connected to J9. For daughter board, please inquire separately.

4.3.23 Ethernet RJ45 Connector, CN5

SOM610 has RGMII interface that supports Gigabit ethernet connection, and DVK supports ethernet connection using Microchips' KSZ9031/KSZ9131 or Realtek's RTL8211E. By default, Microchips' KSZ9031 is mounted, and it can be changed to another chip without any notice depending on the supply and demand situation. Low level ethernet signals must go through a transformer, and DVK is equipped with CN5, an RJ45 standard connector with a built-in 1:1 transformer. The location of CN5 is shown in Fig. 4-39 Location of CN5, RJ45 Connector.

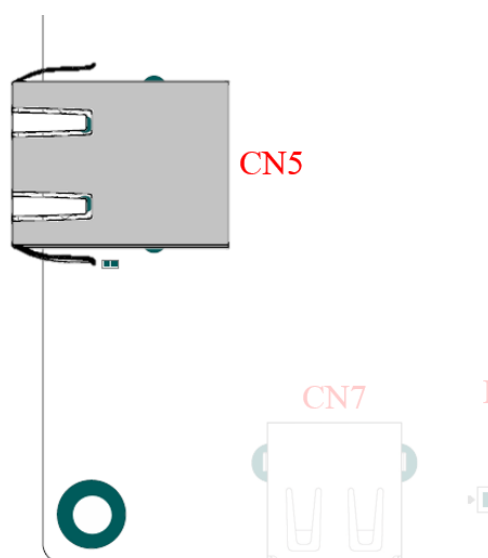


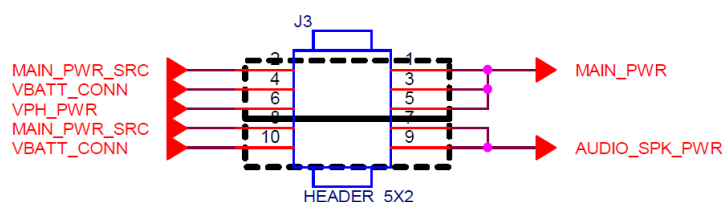
Fig. 4-39 Location of CN5, RJ45 Connector

4.3.24 DVK Main Power Selection Jumper PIN Header, J3

SOM610 DVK has pin header connector J3 for selecting the main power source. The available power sources are as follows and the setting of J3 is shown in Fig. 4-40.

- MAIN_PWR_SRC : See section 4.3.4.2, generated with DC_IN, Default jumper setting
- VBATT_CONN : See section 4.3.25, 4.3.26
- VPH_PWR : Output from SOM610

BD MAIN PWR SELECTION JUMPER



SPK PWR SELECTION JUMPER

Fig. 4-40 Pin Header, J3

Also, the power source supplied to the speaker amplifier inside the audio codec can be selected through J3. The available power sources are as follows.

- MAIN_PWR_SRC : See section 4.3.4.2, generated with DC_IN, Default jumper setting
- VBATT_CONN : See section 4.3.25, 4.3.26, 4.3.17

4.3.25 Battery Power, J2 (Not Implemented)

If you want to use an external battery instead of the battery power source mentioned in section 4.3.26, you can test it by connecting an external battery to J2. By default, the pin header for J2 is not mounted, so to use an external battery, you need to attach the pin header to J2 or connect J2 and the external battery terminal with a wire.

Battery charging/discharging and gauging require further development.

Additional tuning is required as it varies according to battery characteristics, capacity, and frequency of use desired by the user.

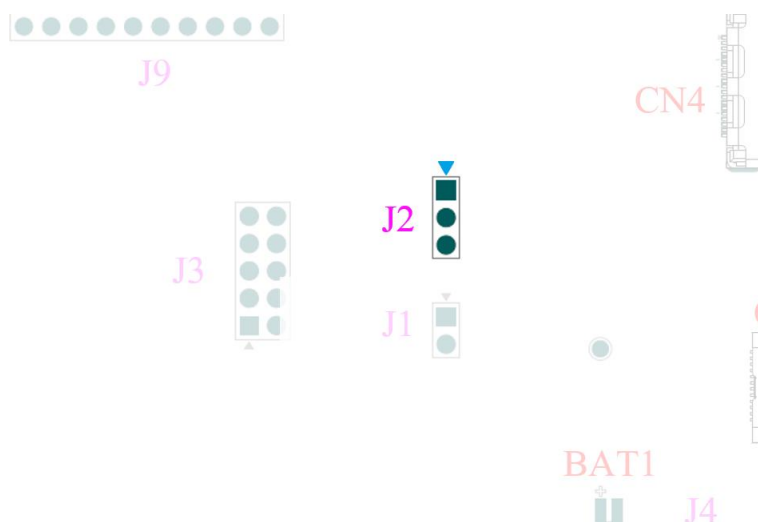


Fig. 4-41 Location of Battery Connector J2

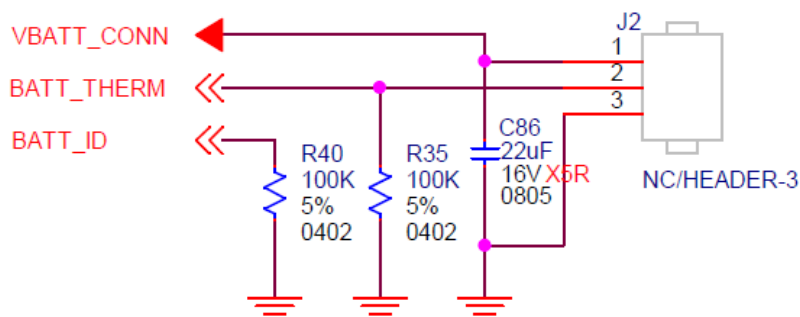


Fig. 4-42 Circuits of Pin Header J2

When connecting an external battery, pay attention to the battery polarity. The position indicated by the blue triangle in Fig. 4-41 is Pin 1, and it increases sequentially in the downward direction. The battery + terminal should be connected to Pin 1, and the battery - terminal should be connected to Pin 3. If there is a thermistor inside the battery and to use the thermistor, it must be connected to Pin 2, and R35 resistor must be removed. Tuning of the thermistor must also be performed.

CAUTION: We are not responsible for any failure caused by the connection of a battery or a separate power supply to J2. The primary fault associated with this is the failure of the SOM610 module and the failure of the carrier board, and the secondary failure is the power adaptor, camera module and all the other components connected to the carrier board, such as the PC or USB hub connected to it. It is not limited to malfunctions, but also includes burns or fires that may occur due to incorrect power connection.

The conditions of the battery available are as follows. For batteries that are randomly connected to the user, battery gauging tuning is required depending on battery characteristics and capacity.

- ✓ Nominal Voltage : 3.7V
- ✓ Type of Battery : Li-Ion or Li-Polymer
- ✓ Capacity : Minimum 1,500mAh, Maximum 4,000 mAh
- ✓ Battery Protection Circuits : 2.8V Undervoltage Cutoff / 4.35V Overvoltage Cutoff

To boot SOM610 DVK system from a well-charged battery (LiB or LiPB) without DC power, you need to connect the battery to SOM610 DVK.

How to properly connect the battery is as follows.

- 1) Removing the jumper from J1; See section 4.3.26
- 2) Connecting the desired external battery to J2

4.3.26 DC to Battery Power Jumper PIN Header, J1

As refer to section 4.3.5, when SW6 is locked to ON, the DC_IN from DC Jack power generates battery power, VBATT_CONN. This means that the system is being powered on.

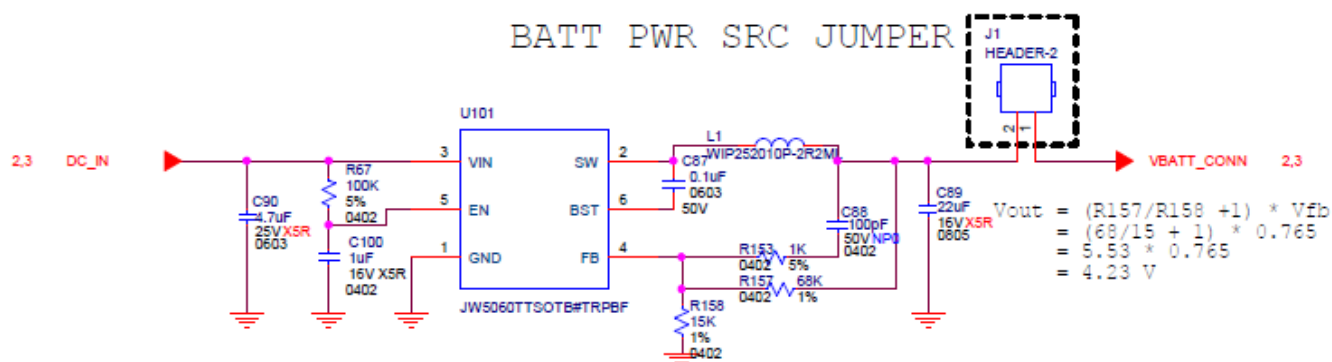


Fig. 4-43 Generating VBATT_CONN from DC_IN

As mentioned in section 4.3.25, if you want to use an external battery without using the external power generated from DC_IN, you must remove the J1 connector's jumper.

The related circuit is shown in Fig. 4-43.

The location of SOM610 DVK's J1 connector is shown in Fig. 4-44.



Fig. 4-44 Location of J1

4.3.27 Summary : Default Board Jumper Setting, J1, J3, J4, J5

The default jumper settings of SOM610 DVK are shown in Fig. 4-45.

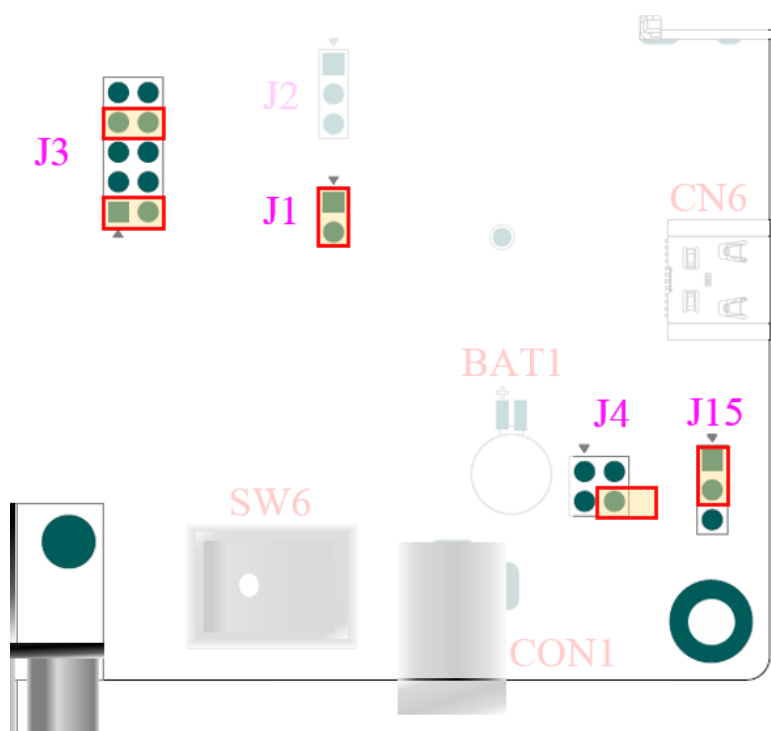


Fig. 4-45 Default Board Jumpers

A brief description of the default settings is as follows, and for details, see the mentioned section.

- J1 : Without external battery, section 4.3.26
- J3 : DC_IN Power Source and 5V Speaker Amp power source, section 4.3.24
- J4 : Boot Mode, section 4.3.6
- J15 : USB_CC1, section 4.3.7